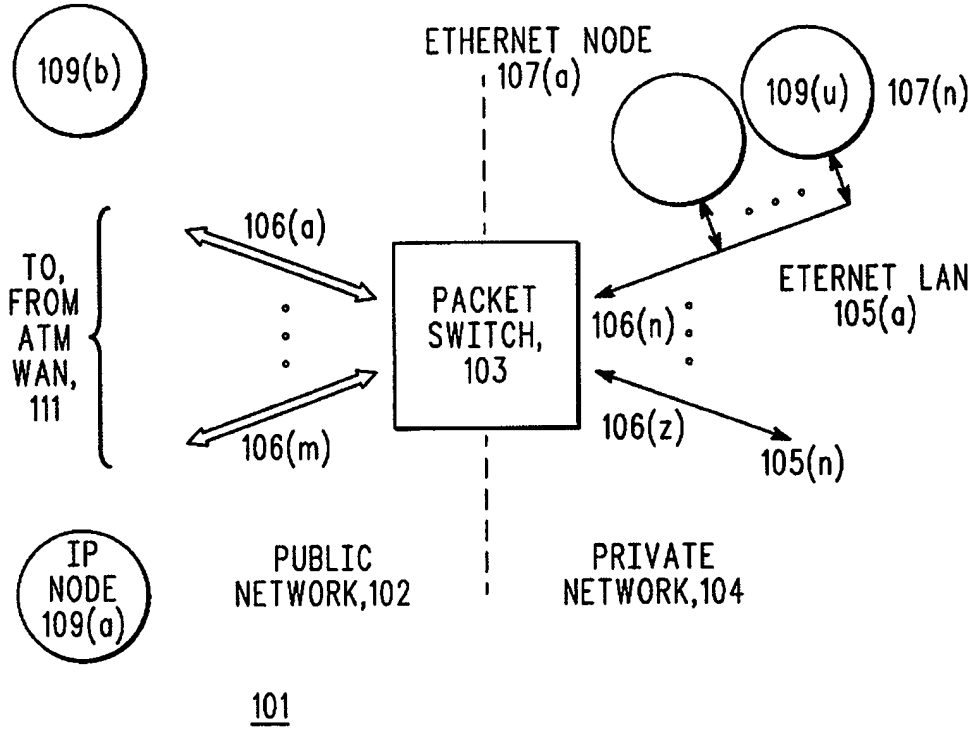
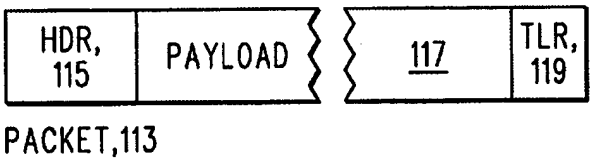




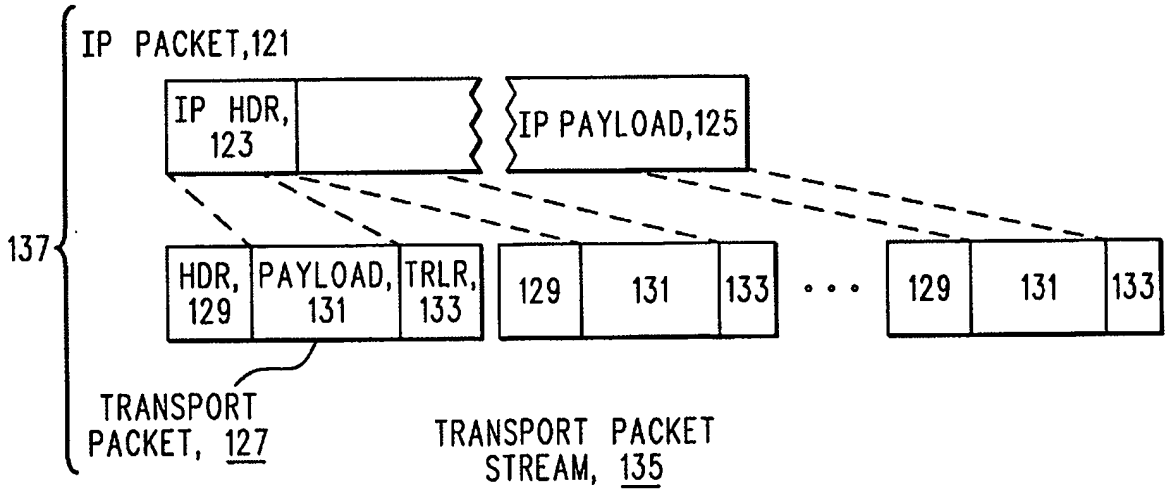


Fig.1
(PRIOR ART)

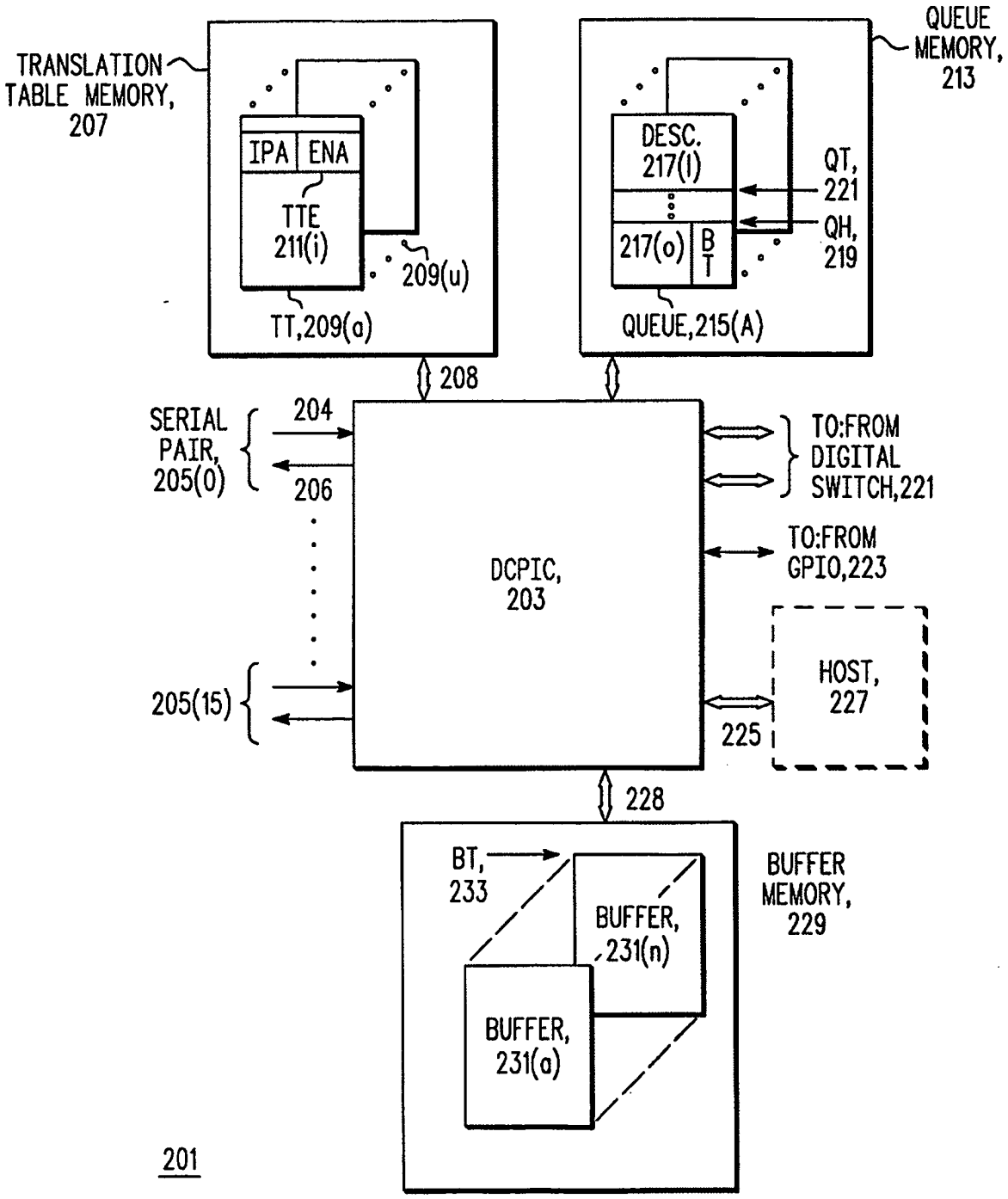


Fig.2

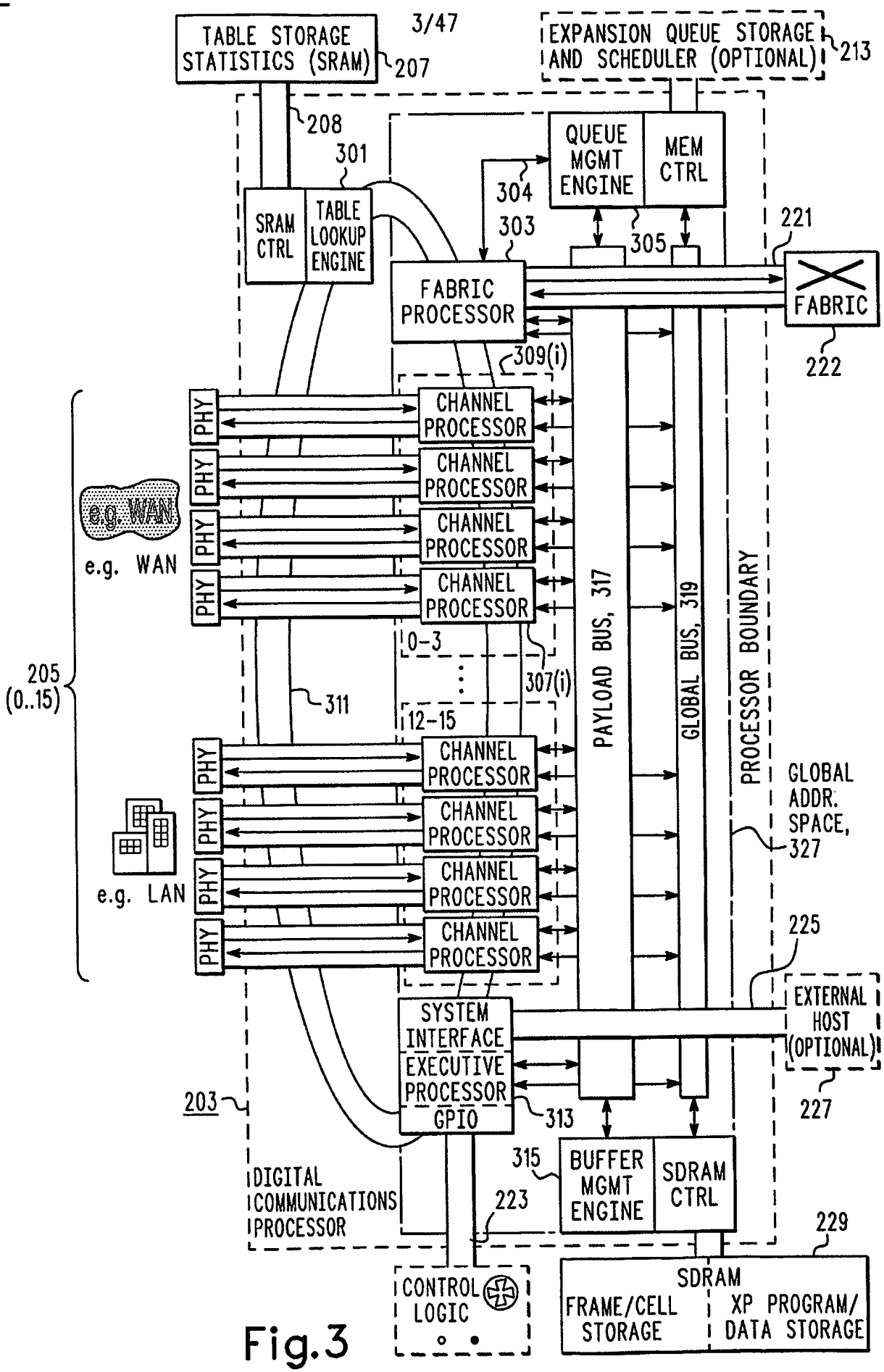


Fig.3

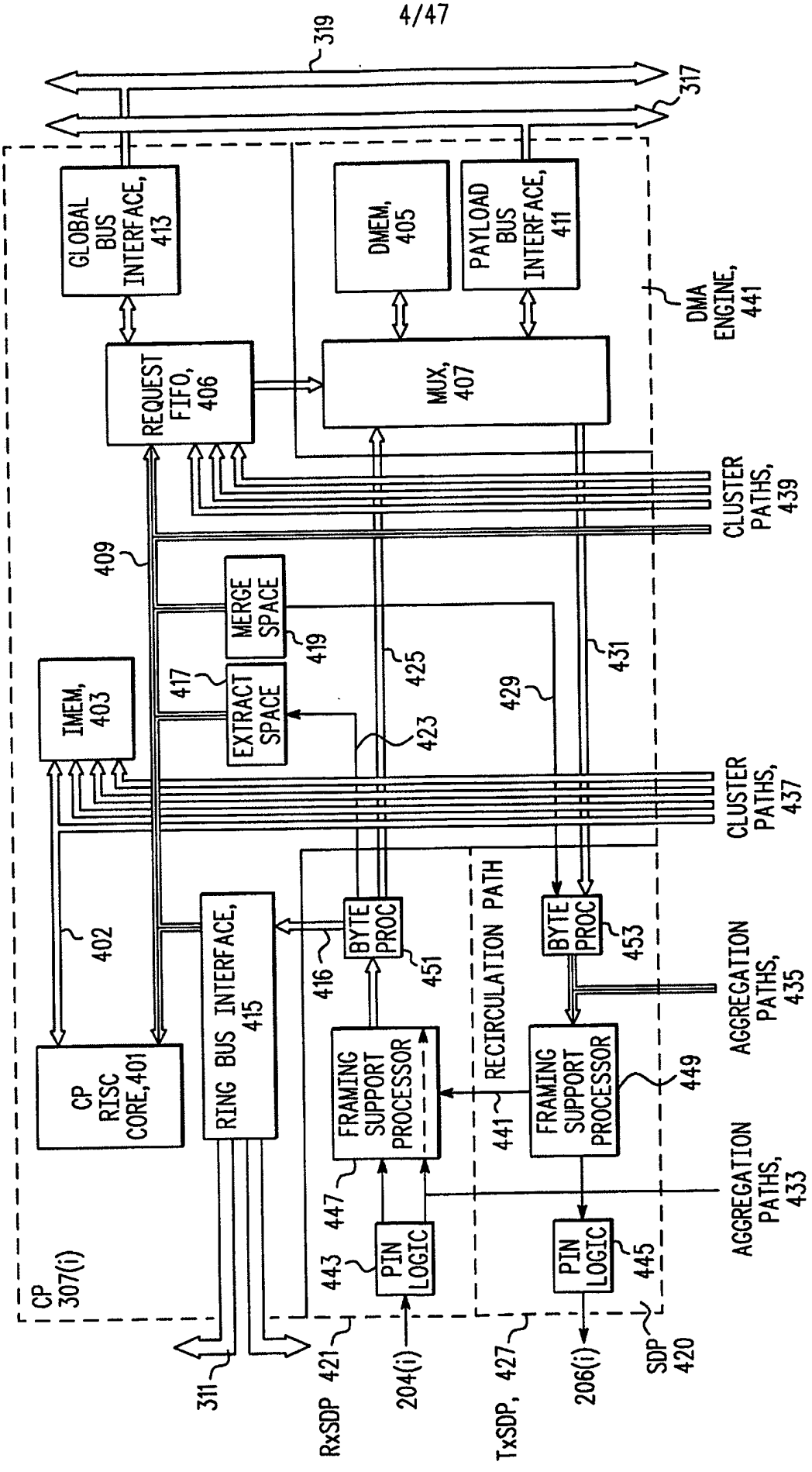
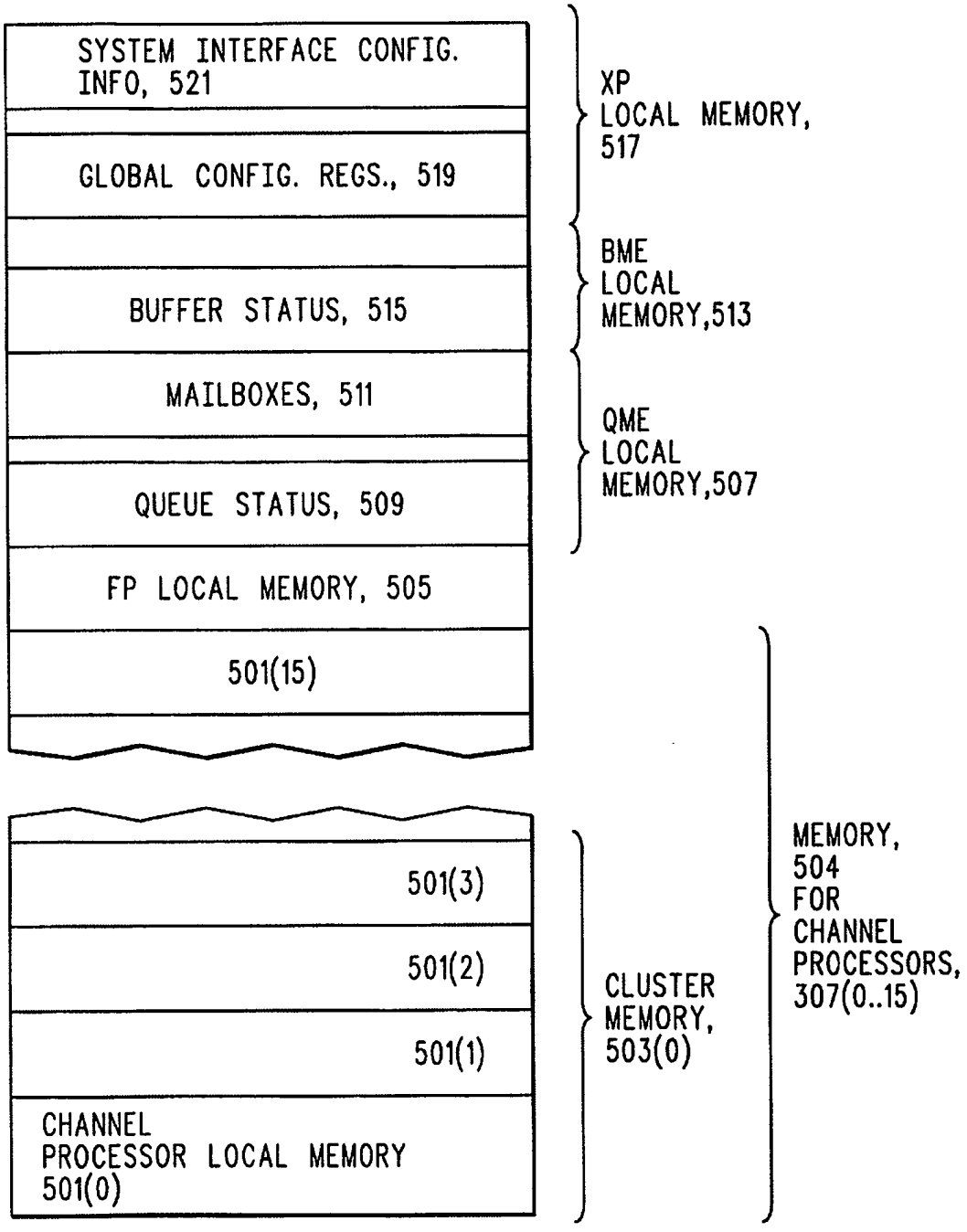


Fig.4



321

Fig.5

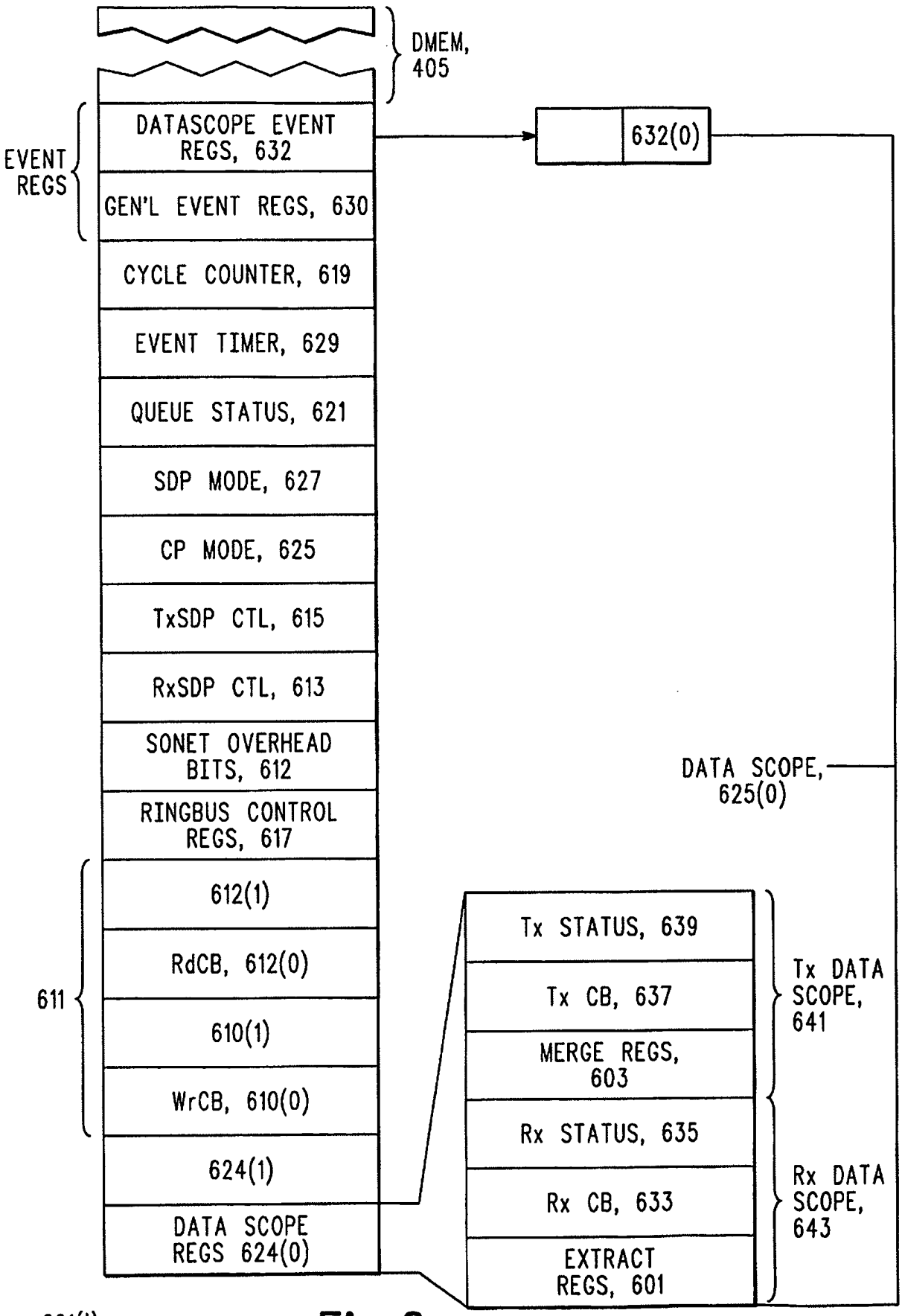


Fig.6

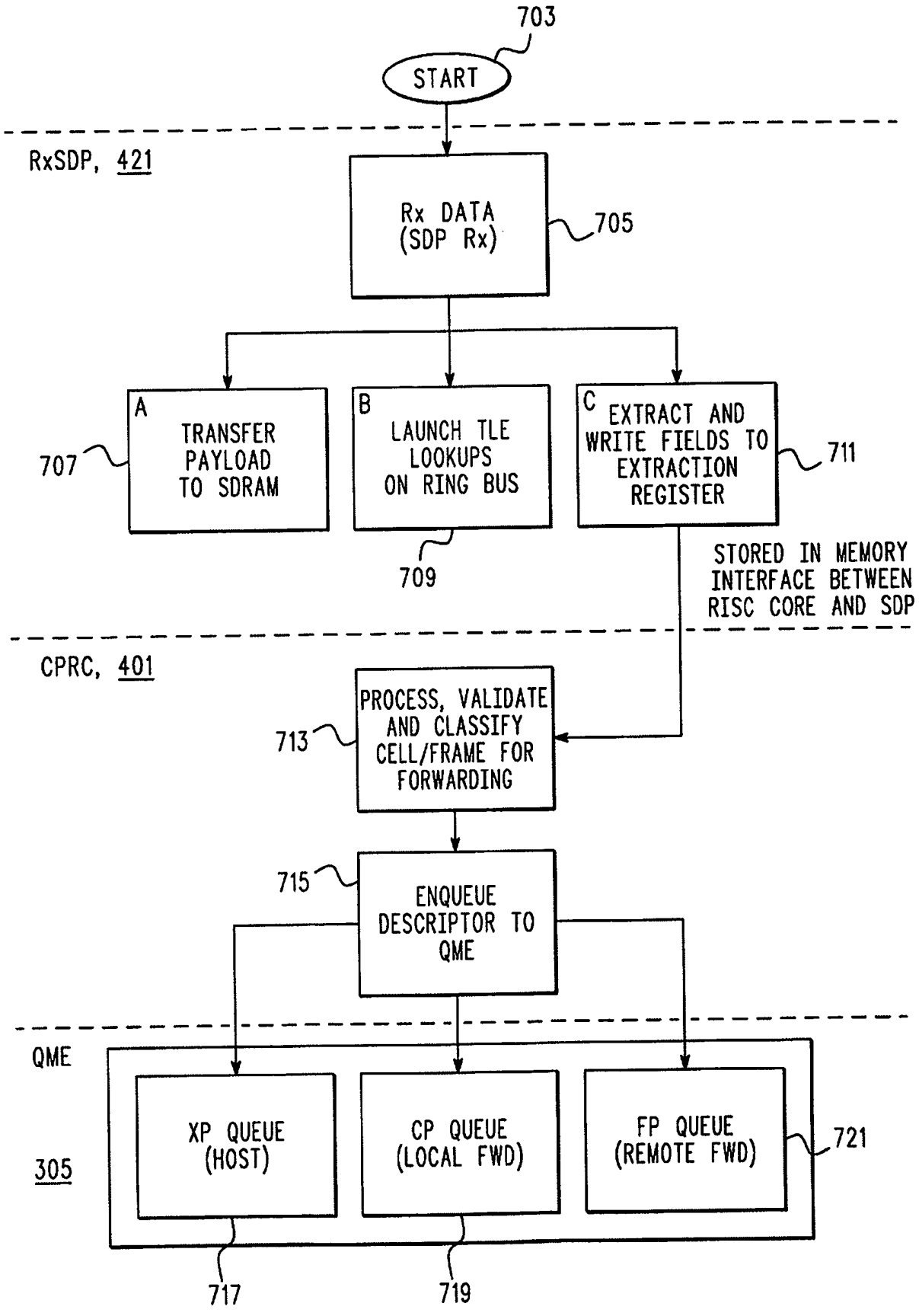


Fig.7

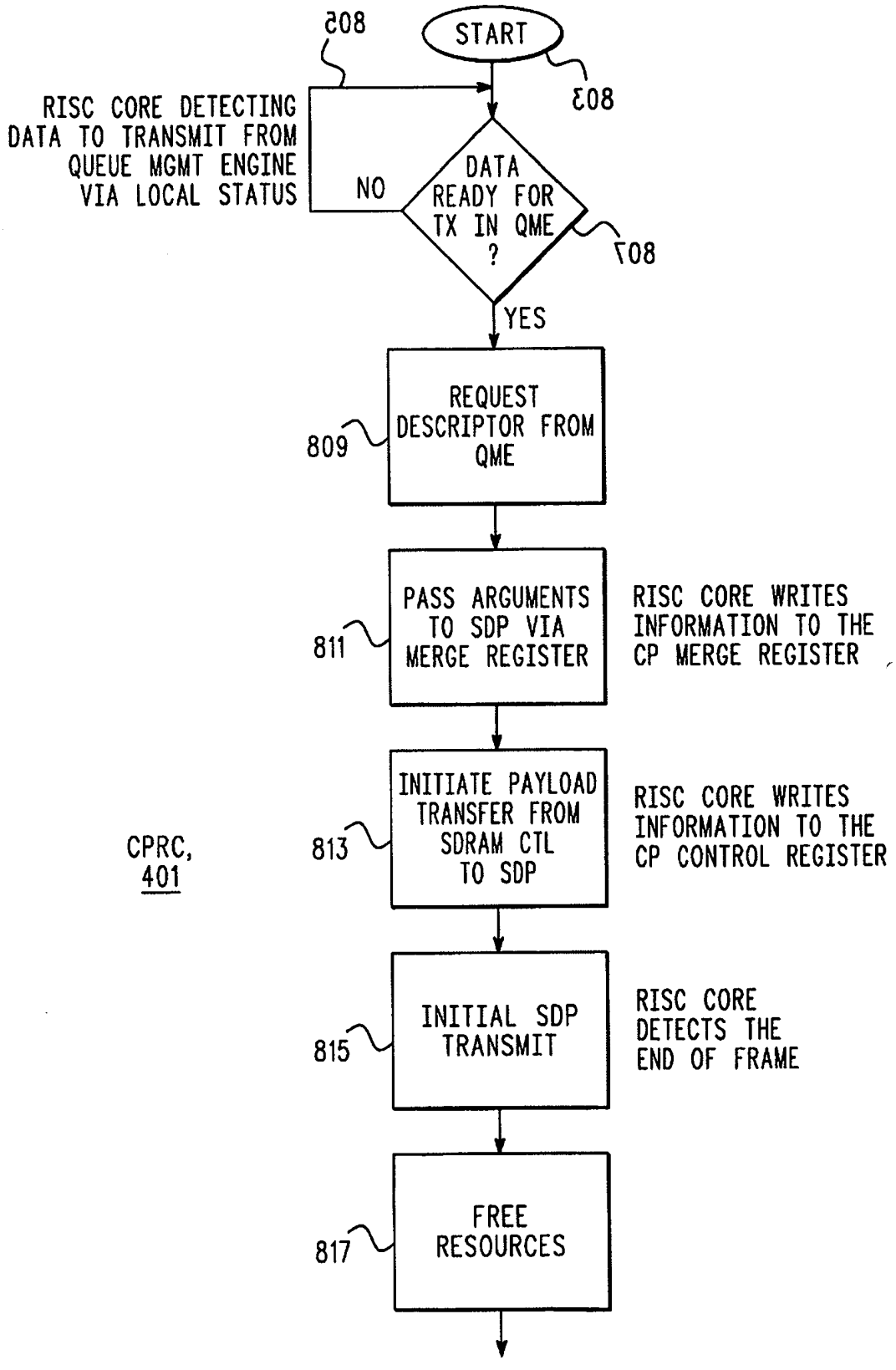


Fig.8

OWN, 935	L5:L0 937	BUSY, 941

635

BTAG, 933			
OFFSET, 931			
Av, 929	NR, 927	Err, 925	OWN, 921
SDPST, 915	EOP, 927	BCTL, ST 919	
LENGTH, 911			
BUFFER POOL NO, 909			
DMEM DMAADDR, 907			
TxRcy ADDR., 905			
RxRcy ADDR., 903			
DMEM BYTE ADDR., 901			

RxCBCTL, 913

633

Fig.9

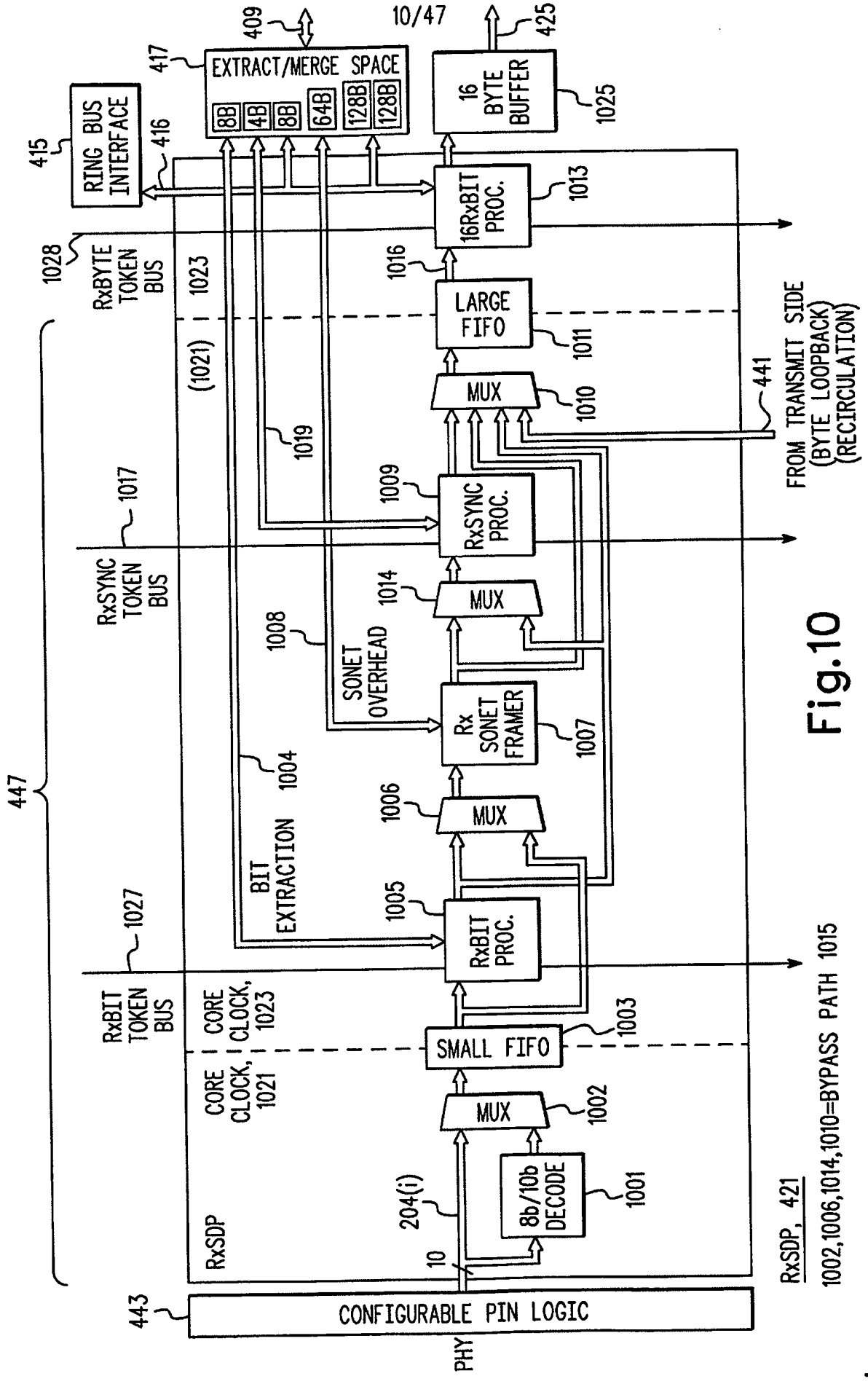


Fig.10

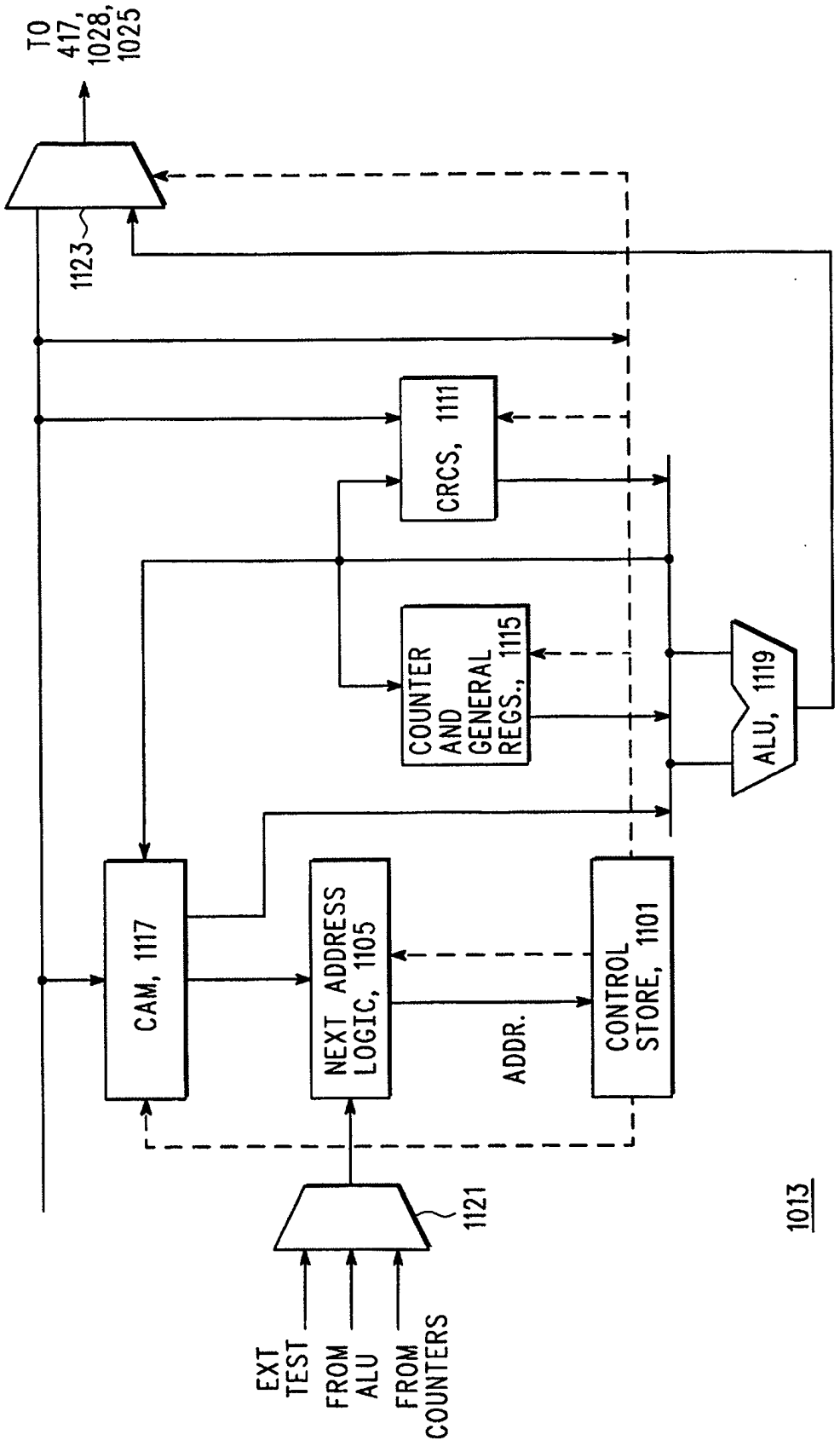


Fig. 11

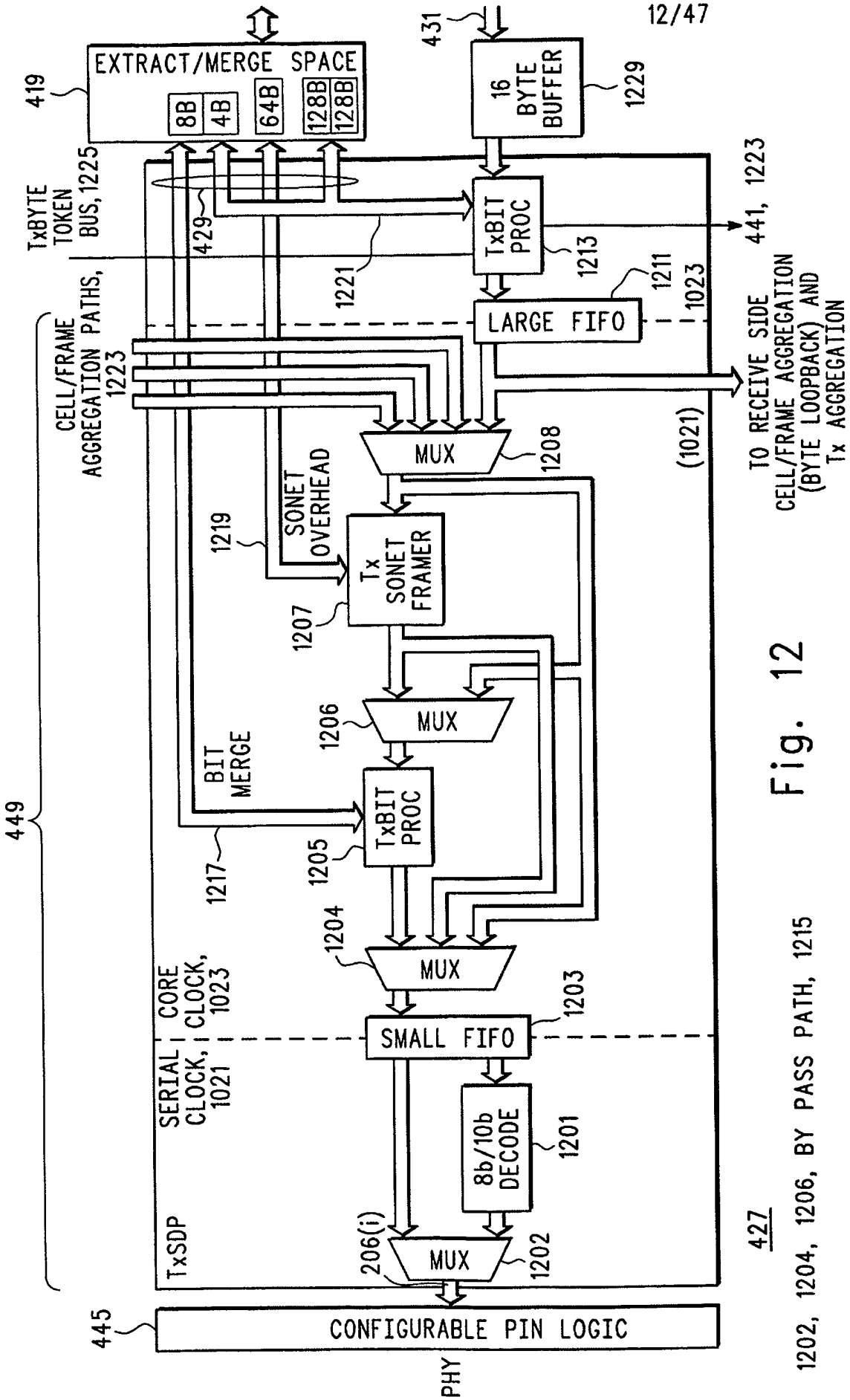


Fig. 12

1202, 1204, 1206, BY PASS PATH, 1215

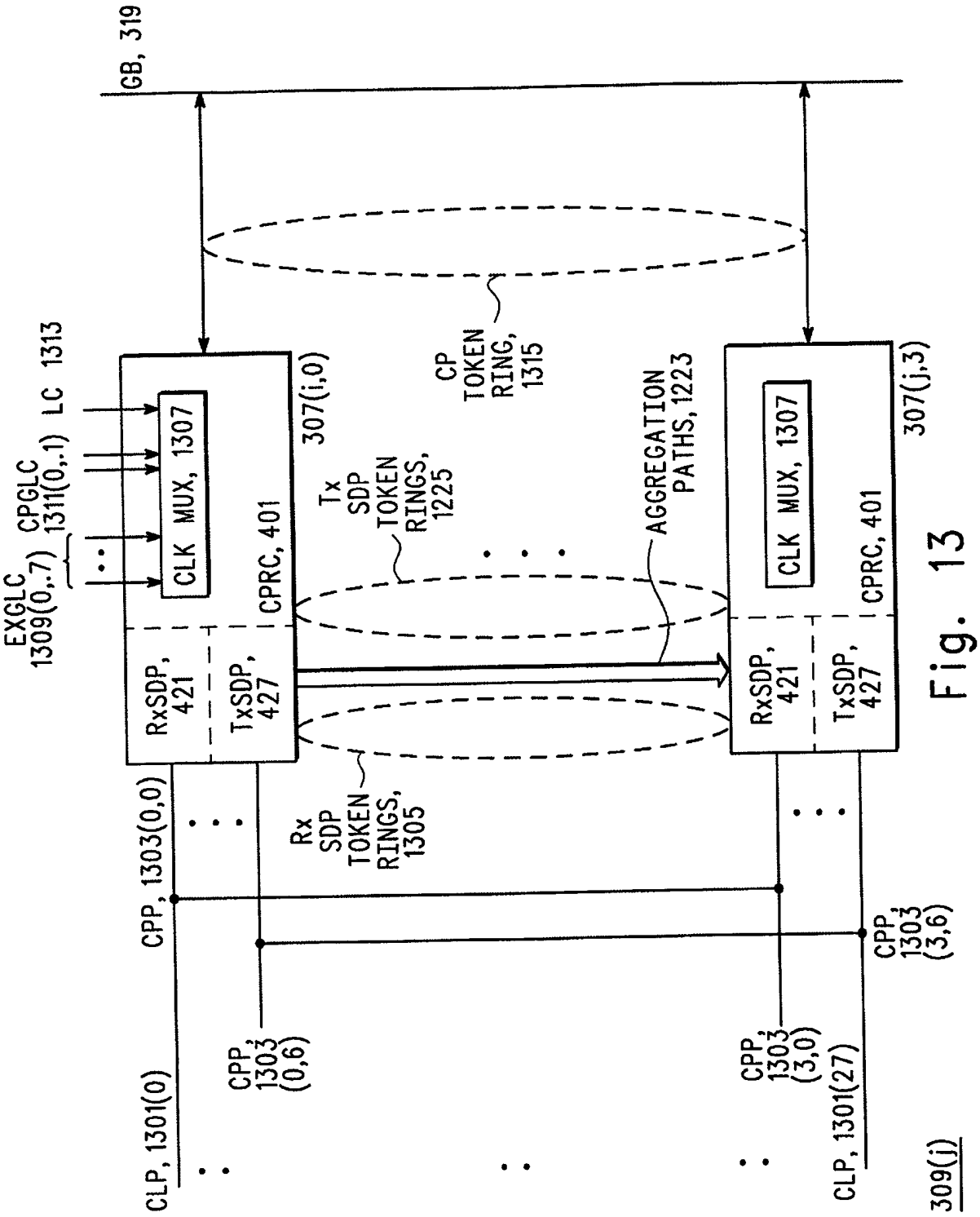


Fig. 13

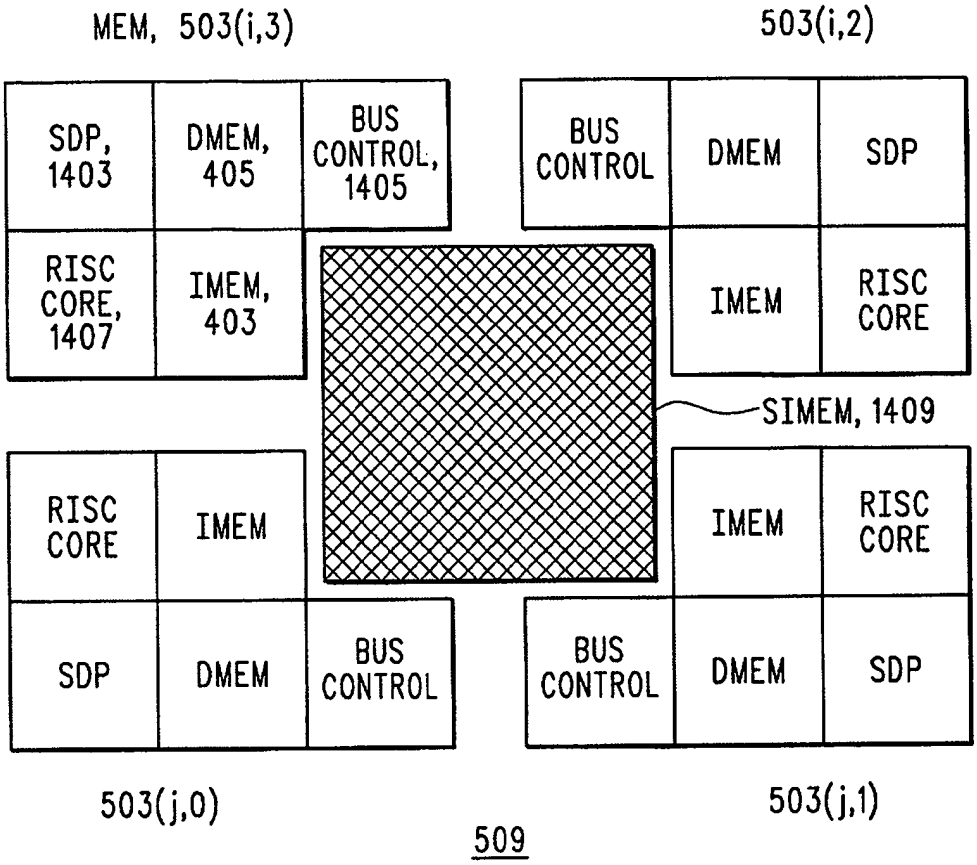


Fig. 14

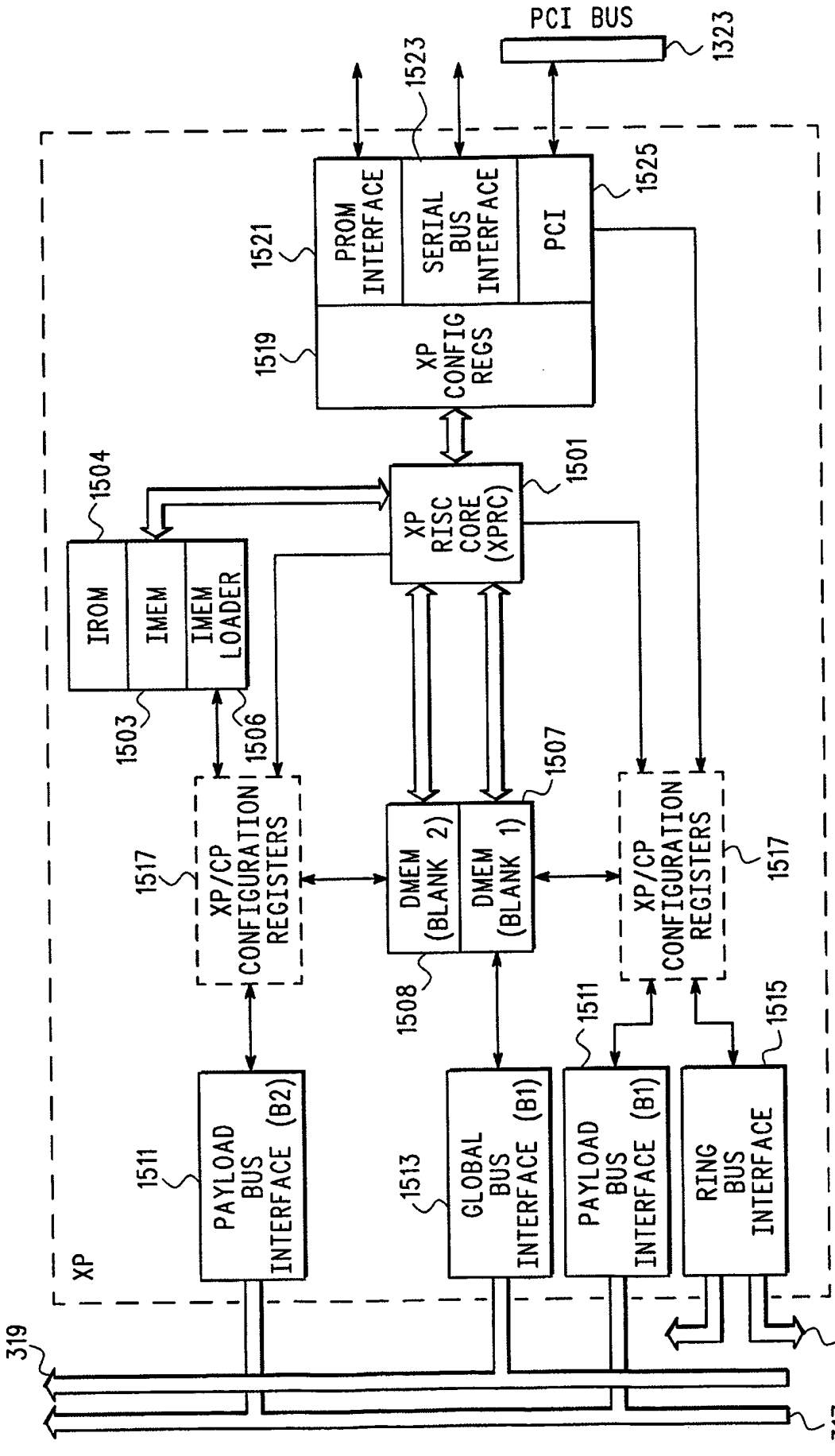


Fig. 15

Replacement Sheet

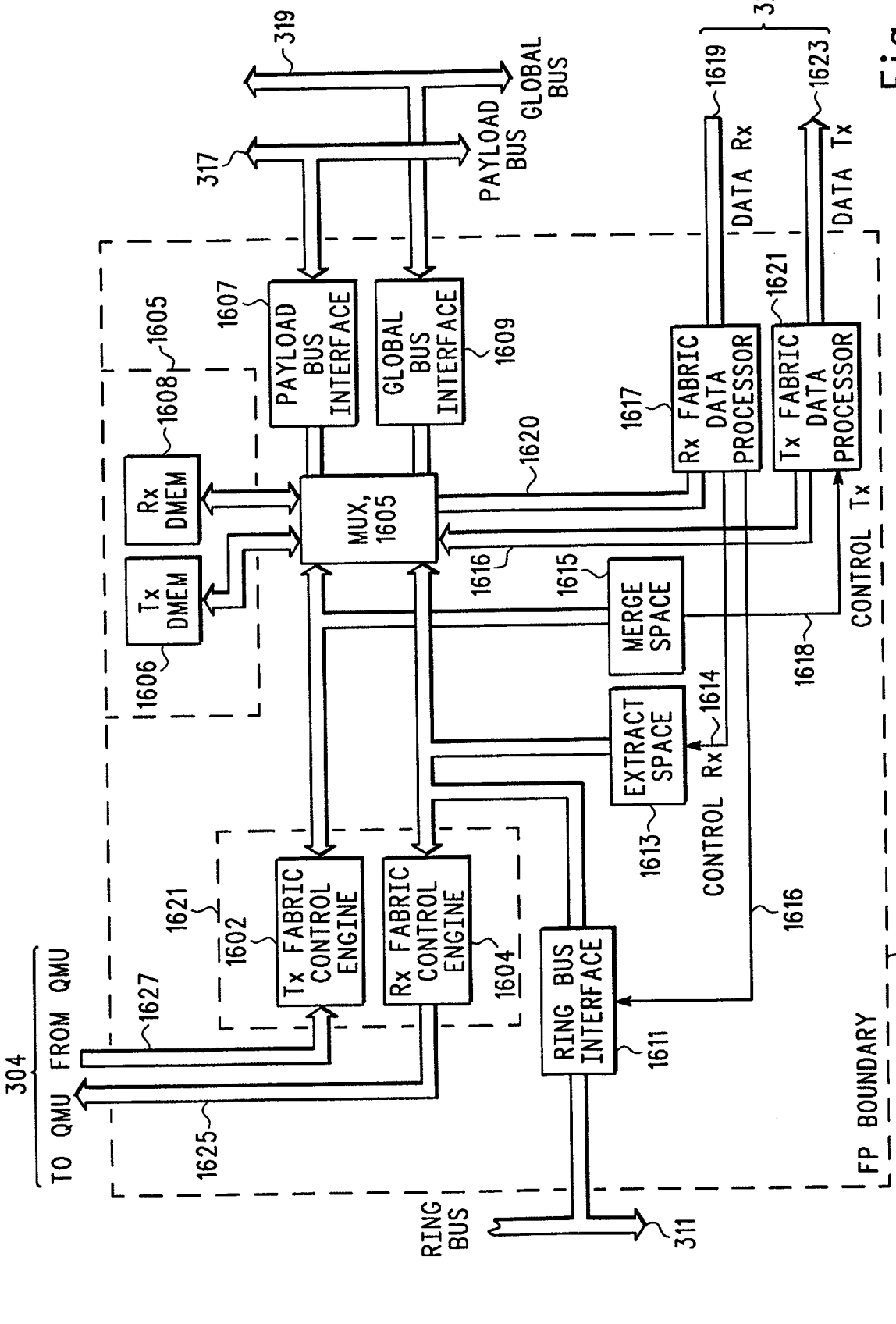


Fig. 16

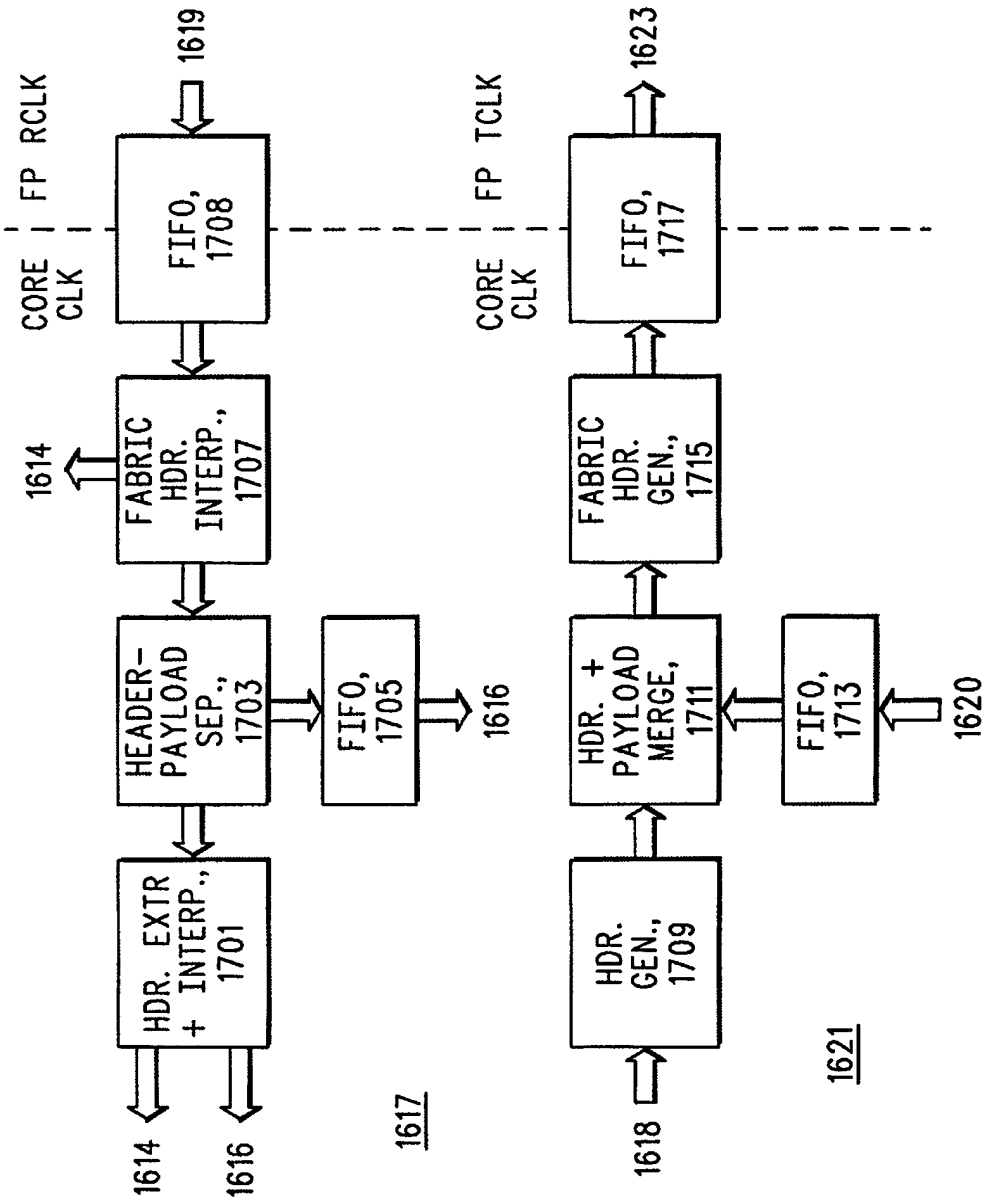


Fig. 17

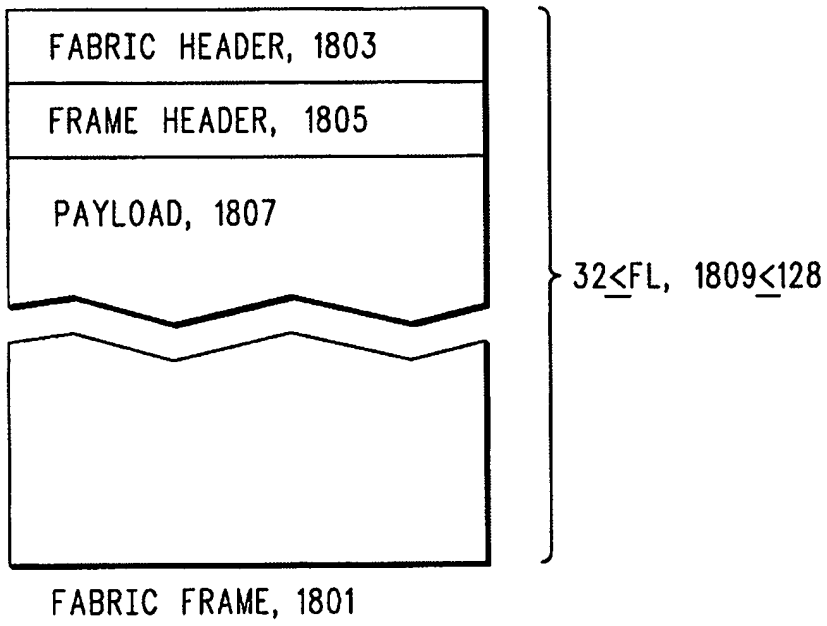


Fig. 18

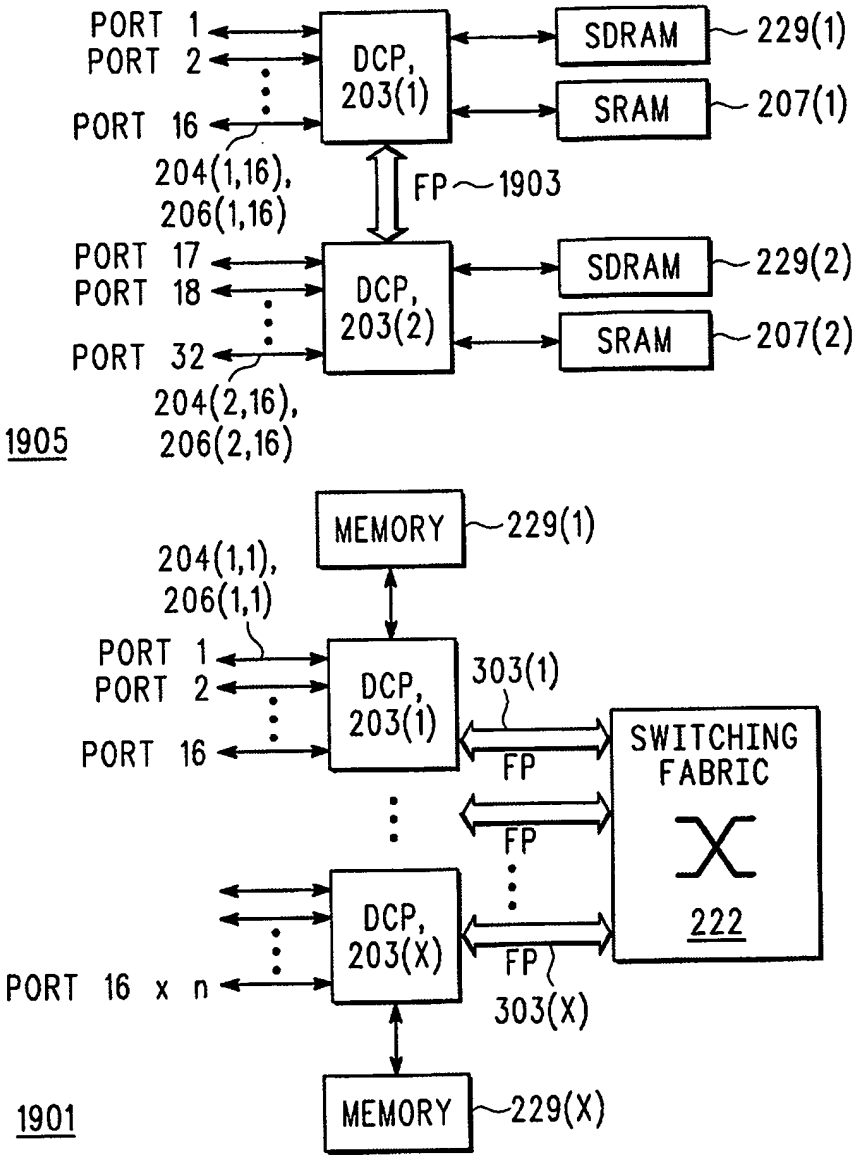


Fig. 19

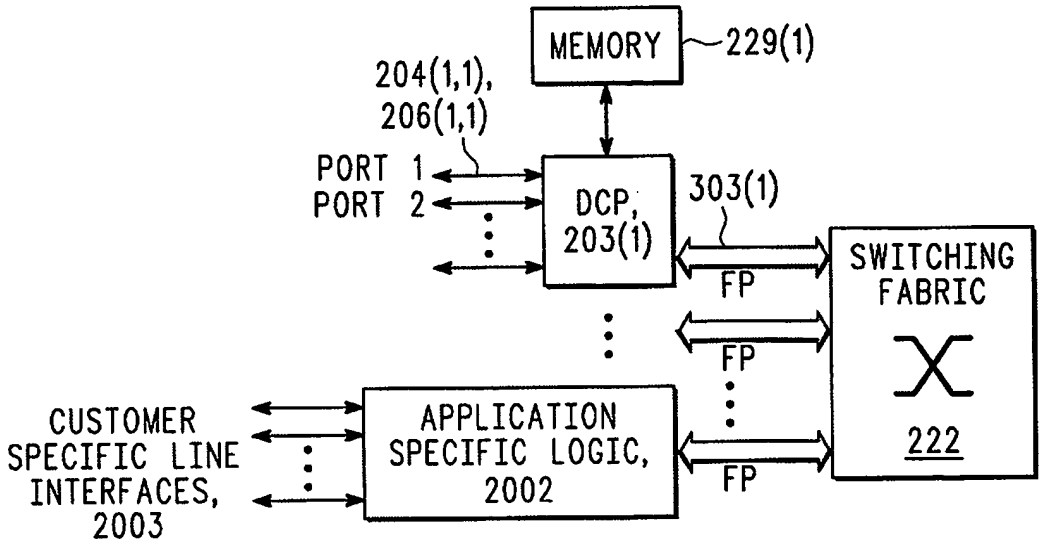


Fig. 20

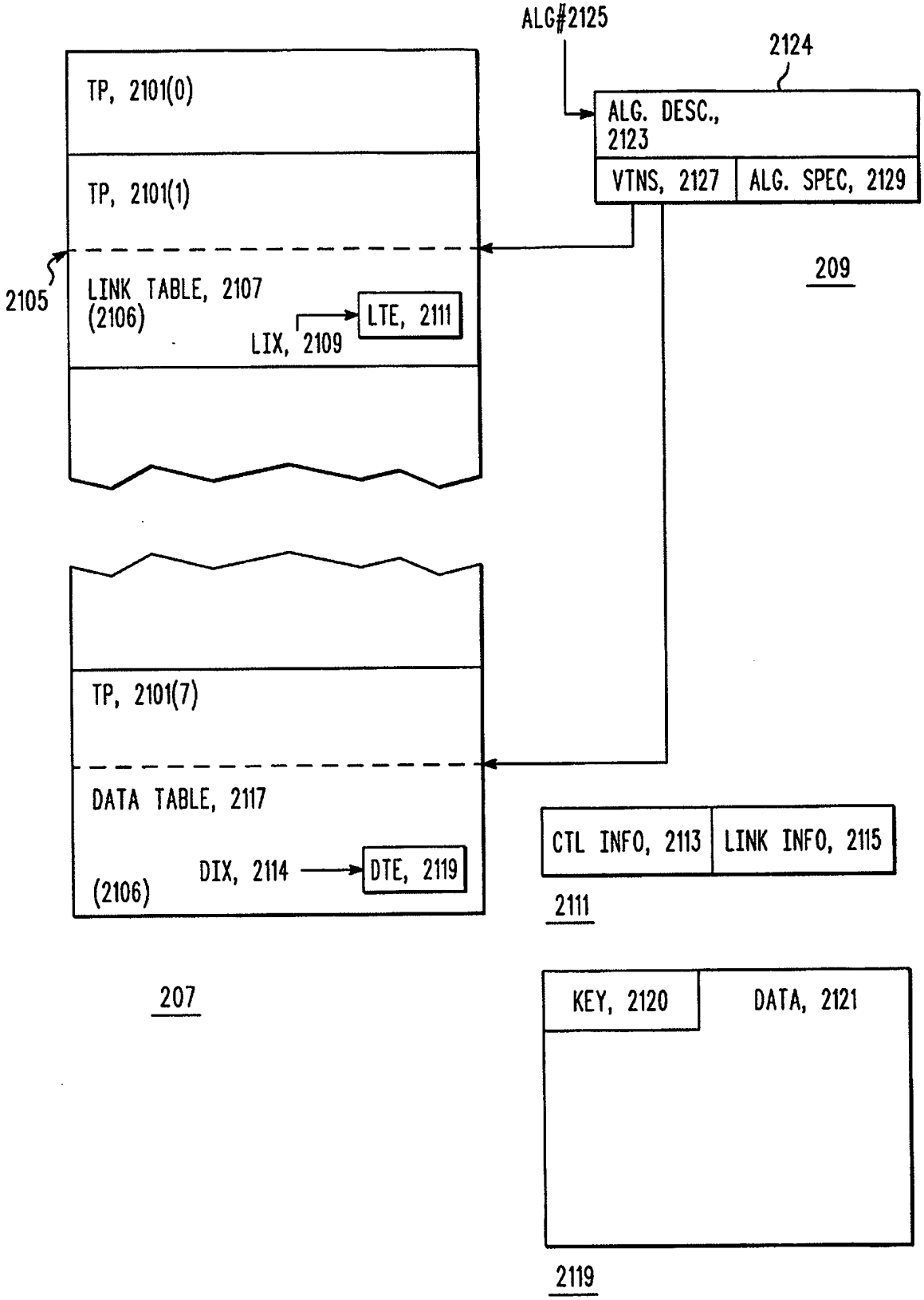


Fig. 21

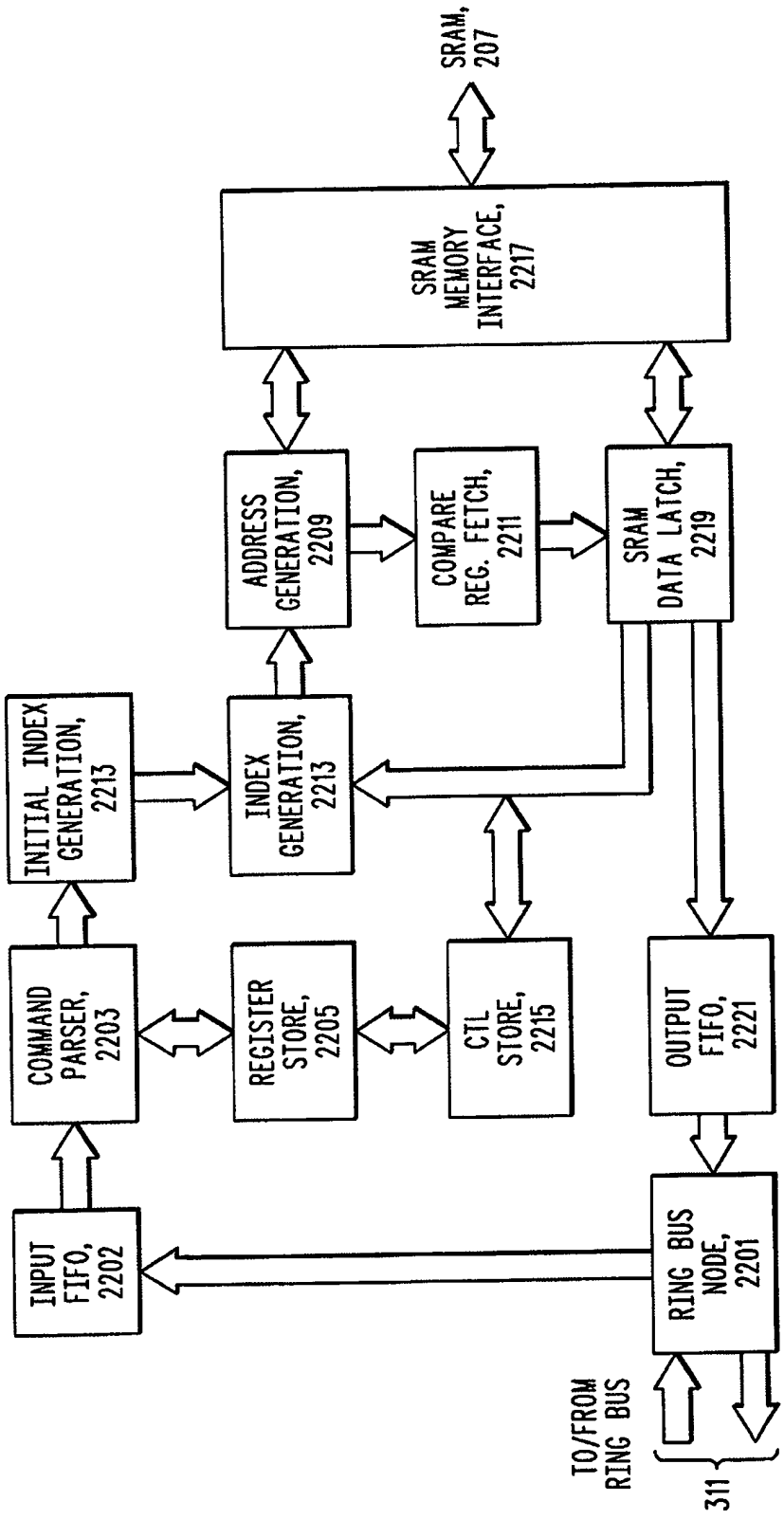


Fig. 22

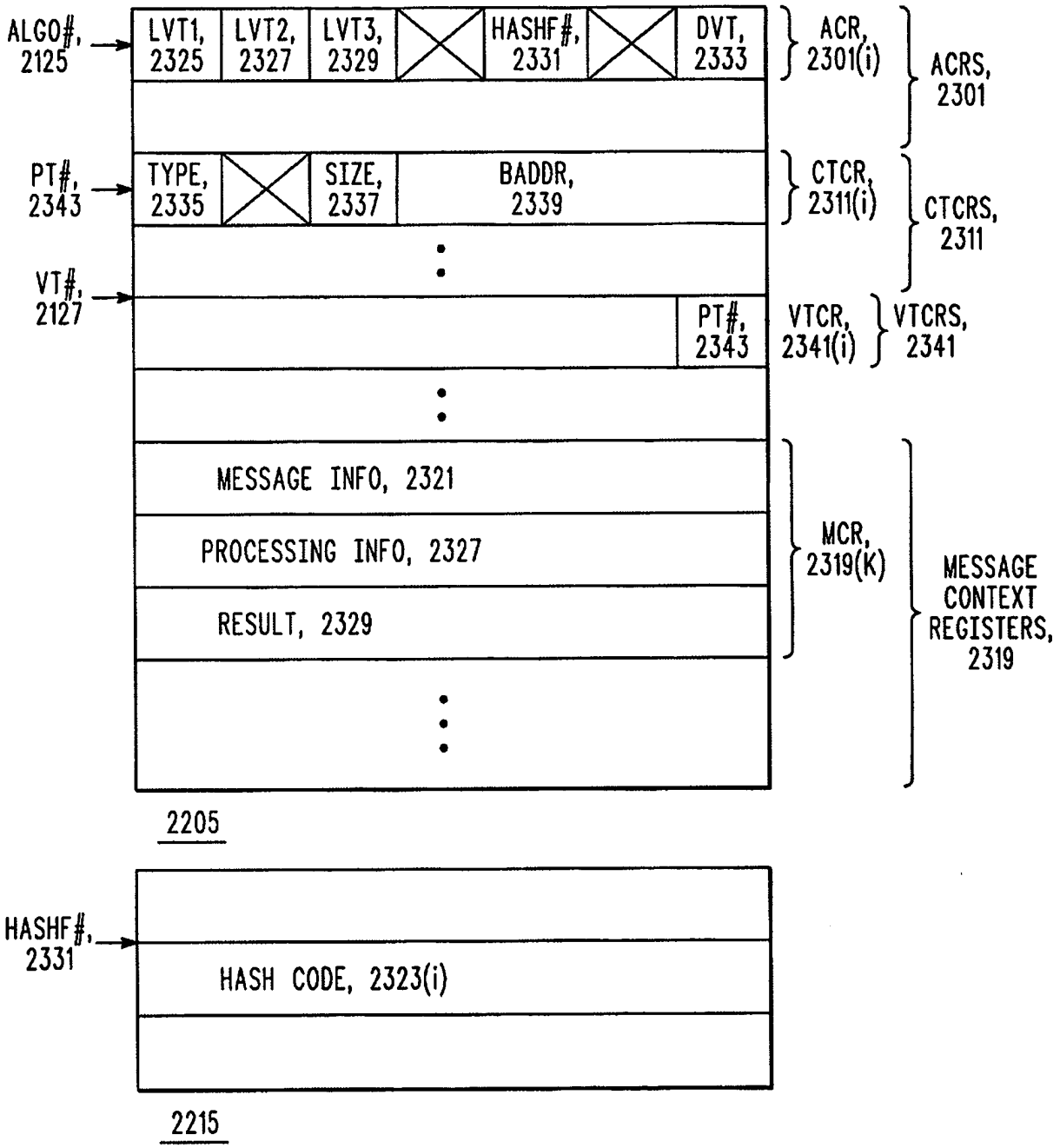


Fig. 23

	COMMAND	COMMAND ID	RETURN DATA	DESCRIPTION	
2421	WRITE(VTABLE#,INDEX, MASK,DATA,OFFSET, LENGTH)	0X2	NONE	WRITE DATA INTO A VIRTUAL TABLE AT INDEX.	2401
2421	READ(VTABLE#,INDEX, OFFSET,LENGTH)	0X3	DATA	READS DATA FROM A VIRTUAL TABLE.	2403
2423	FINDW(ALG#,KEY)	0X6	PHYSICAL TABLE, INDEX, ERROR	FINDS A KEY USING ALG#. SETS RING BUS ERROR FLAG IF KEY IS NOT FOUND.	2405
2423	FINDW(ALG#,KEY,DATA, OFFSET,LENGTH)	0X4	PASS/FAIL, INDEX, ERROR	WRITES DATA INTO A TABLE USING A KEY. SETS RING BUS ERROR FLAG IF THE KEY IS NOT FOUND.	2407
2423	FINDR(ALG#,KEY,DATA, OFFSET,LENGTH)	0X5	PASS/FAIL, INDEX, DATA	READS LENGTH DWORDS OF DATA FROM A VTABLE# USING A KEY AT OFFSET DWORDS. SETS RING BUS ERROR FLAG IF THE KEY IS NOT FOUND	2409
2425	XOR(VTABLE#,INDEX, DATA/PCRC,OFFSET, MASK,CRC,LAST)	0X1	NONE OR CRC IN CRC MODE	XOR'S UP TO A 32 BIT VALUE TO OFFSET. ONLY MASKS OF UP TO FOUR CONSECUTIVE BYTES ARE VALID. A SPECIAL MODE EXISTS FOR CRC CALCULATIONS.	2411
2425	ADD(VTABLE#,INDEX, DATA,OFFSET,MASK)	0X7	NONE	ADDS UP TO A 32-BIT VALUE TO OFFSET. ONLY MASKS OF UP TO FOUR CONSECUTIVE BYTES ARE VALID.	2413
2427	WRITEREG(REG-ADDR, DATA)	0X0,0x10	NONE	WRITE DATA TO TLE REGISTER AT REG_ADDR.	2415
2427	READREG(REG_ADDR, DATA)	0X0,0x11	DATA	READ DATA FROM TLE REGISTER AT REG_ADDR.	2417
2427	ECHO(DATA)	0X0,0x04	DATA	RETURN DATA FROM TLE FOR TEST PURPOSES	2419
2427	NOP()	0X0,0x05	NONE	INSERTS A NOP INTO THE TLE PIPE	2420

Fig. 24

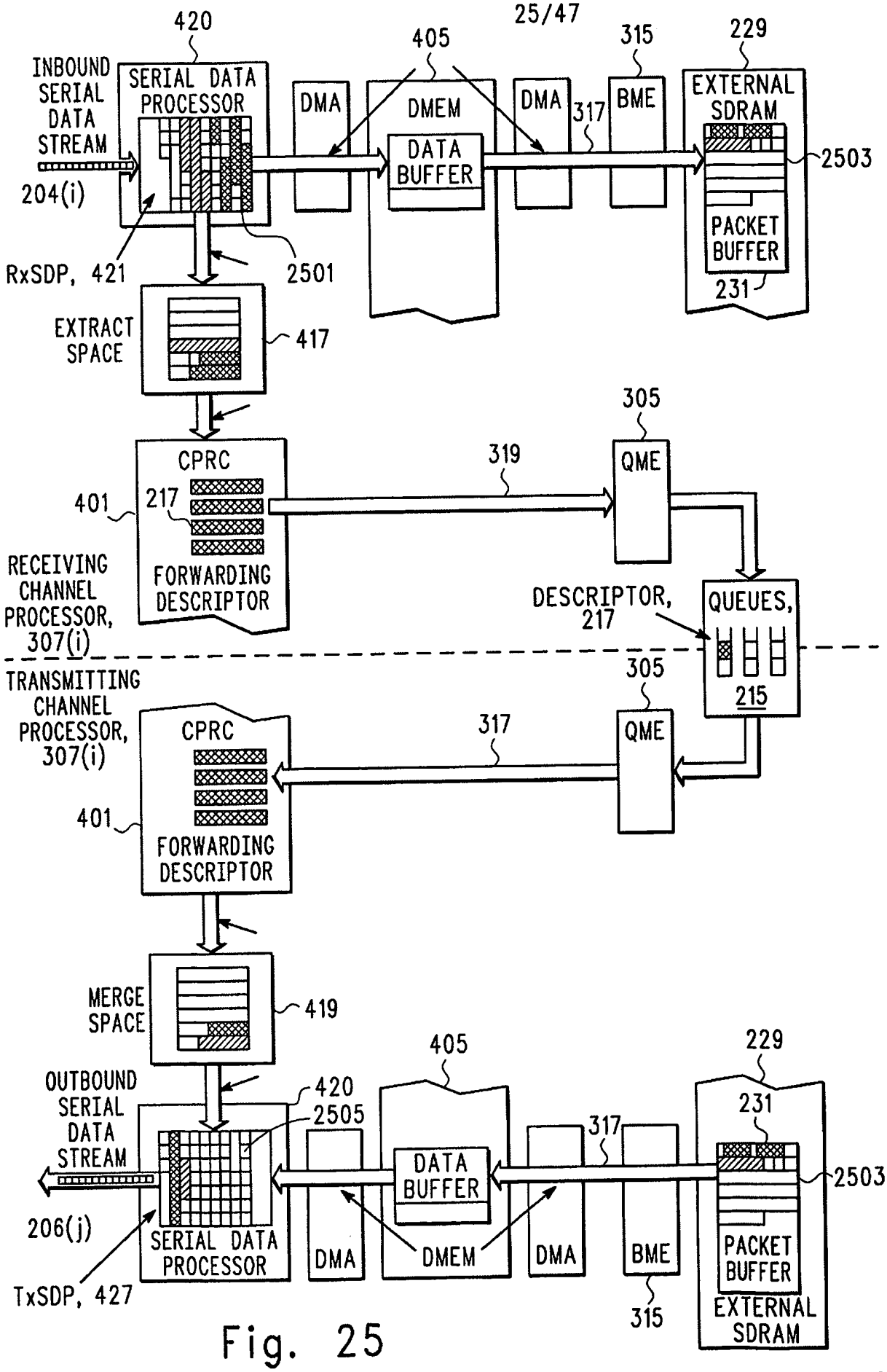
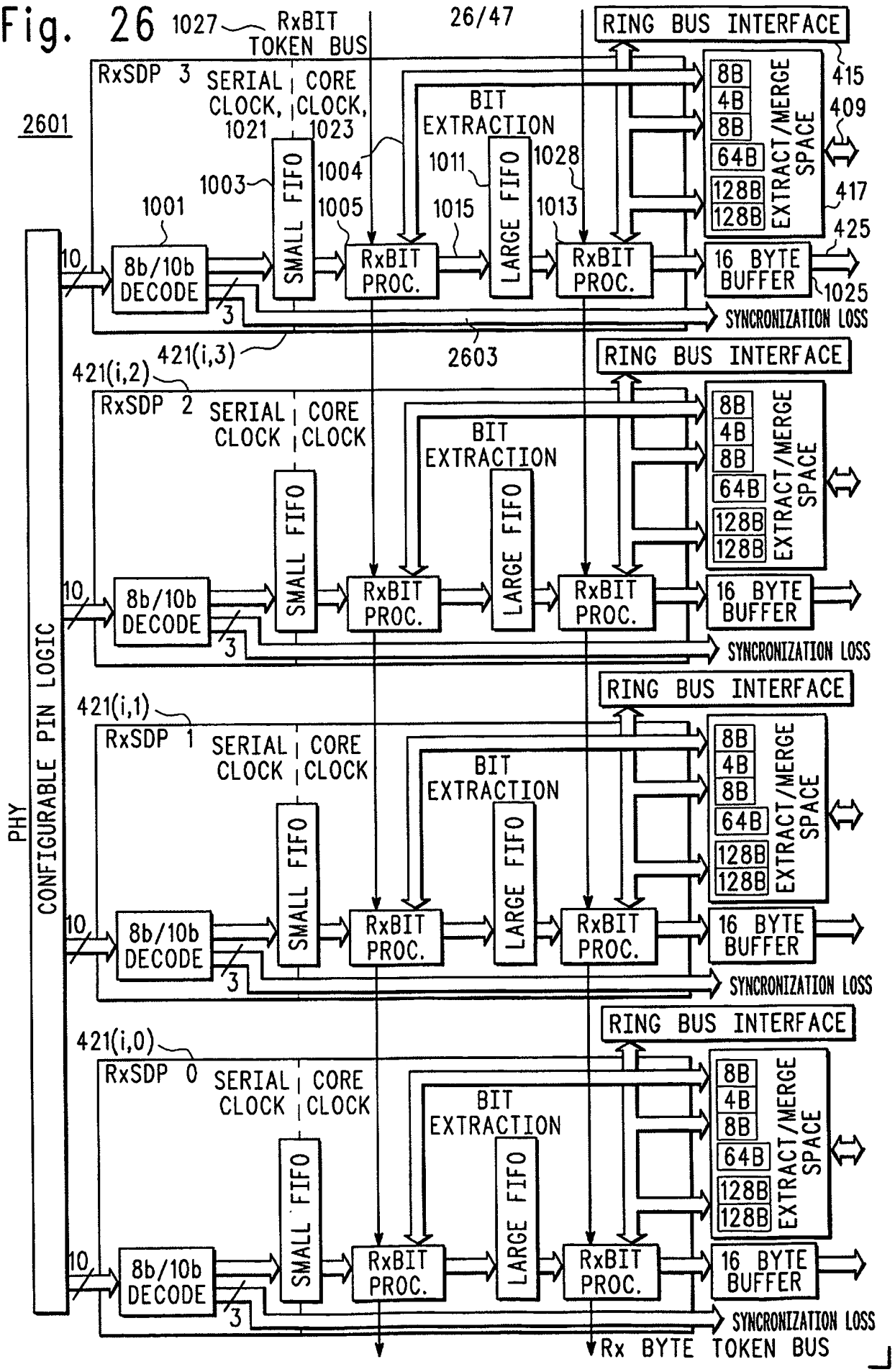
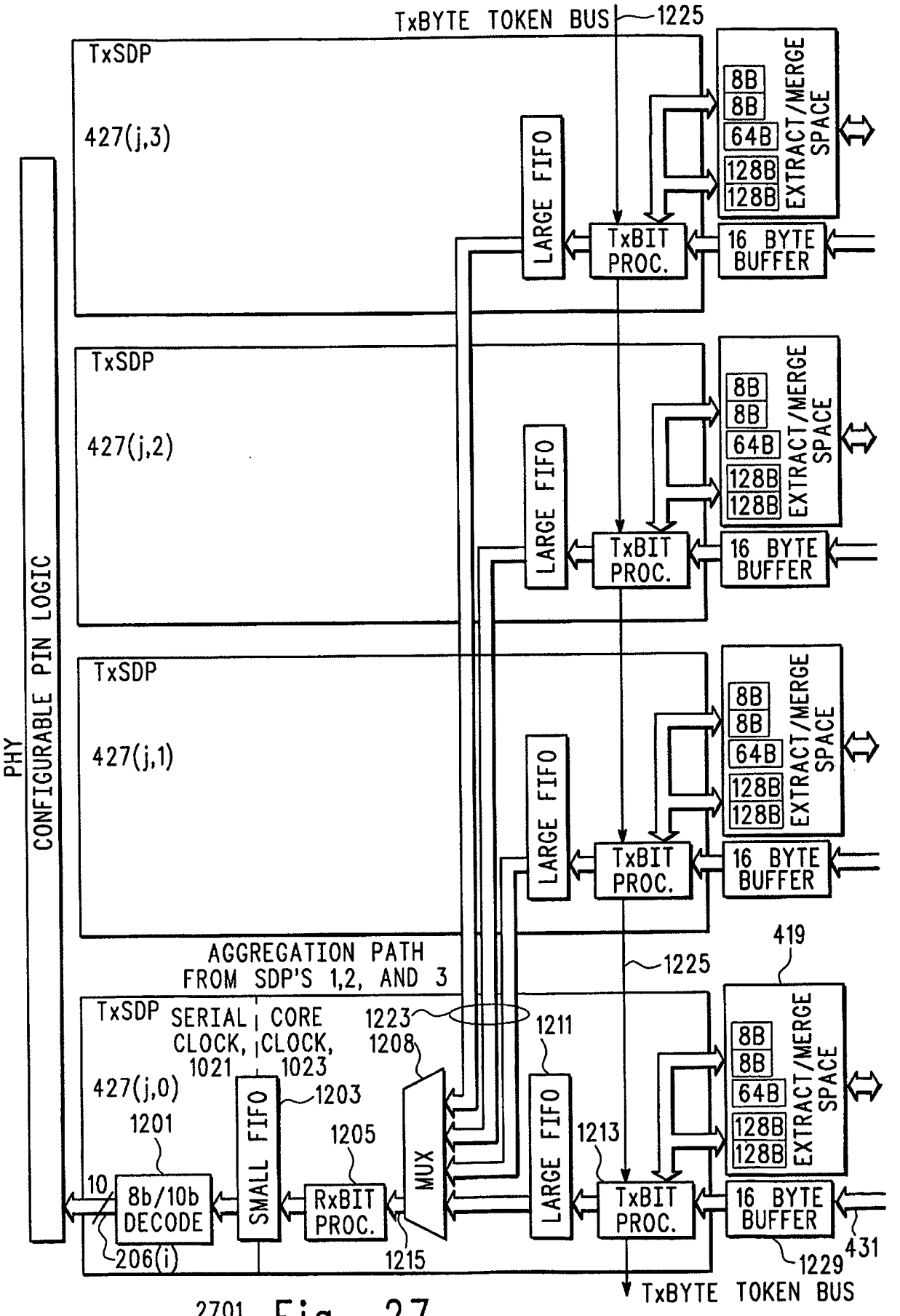


Fig. 25

Fig. 26





2701 Fig. 27

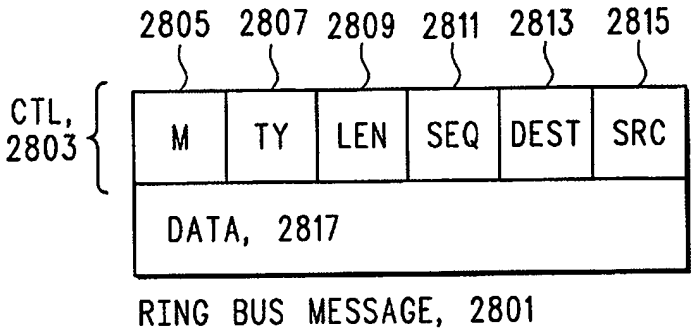
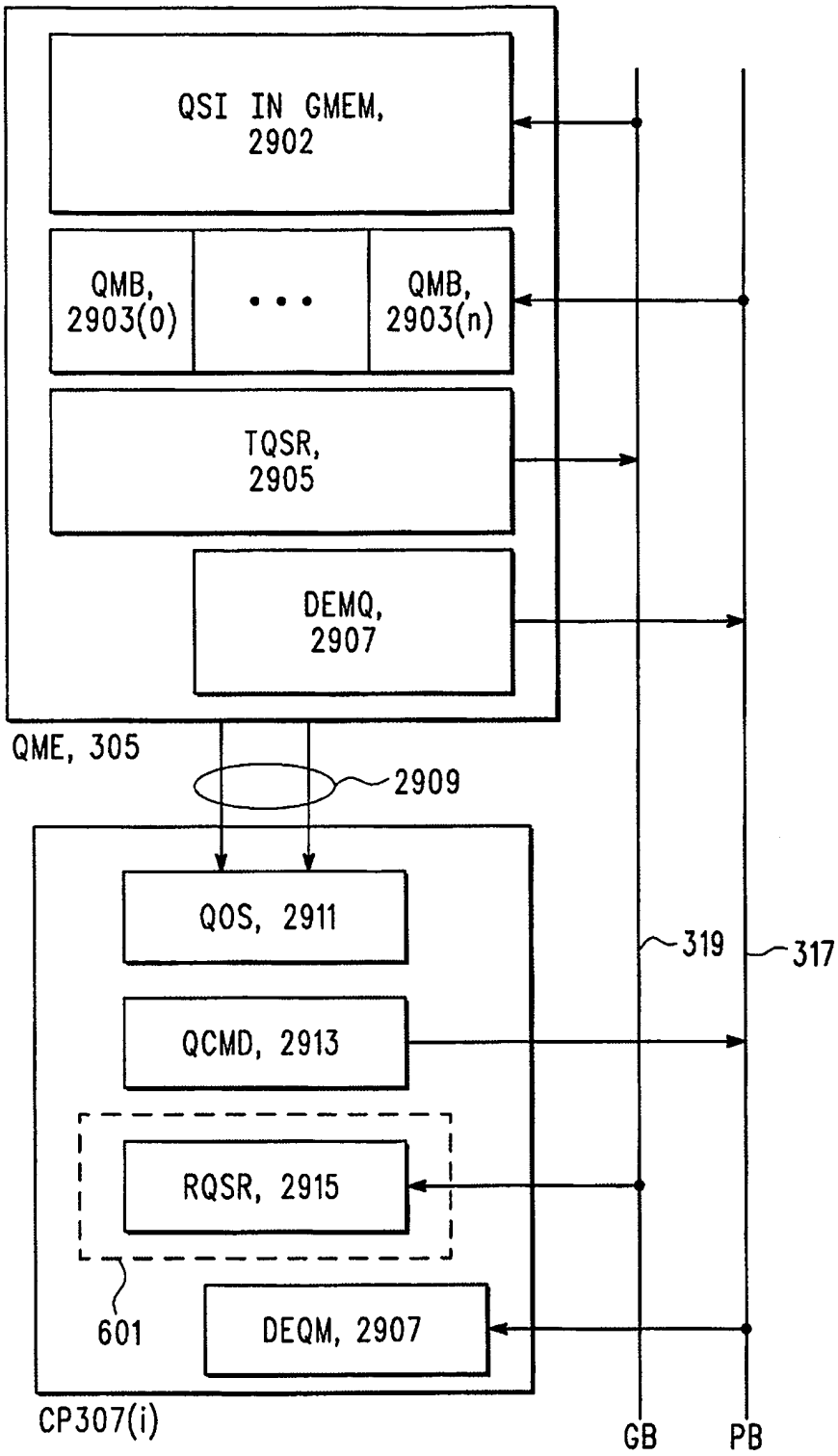


Fig. 28



2901

Fig. 29

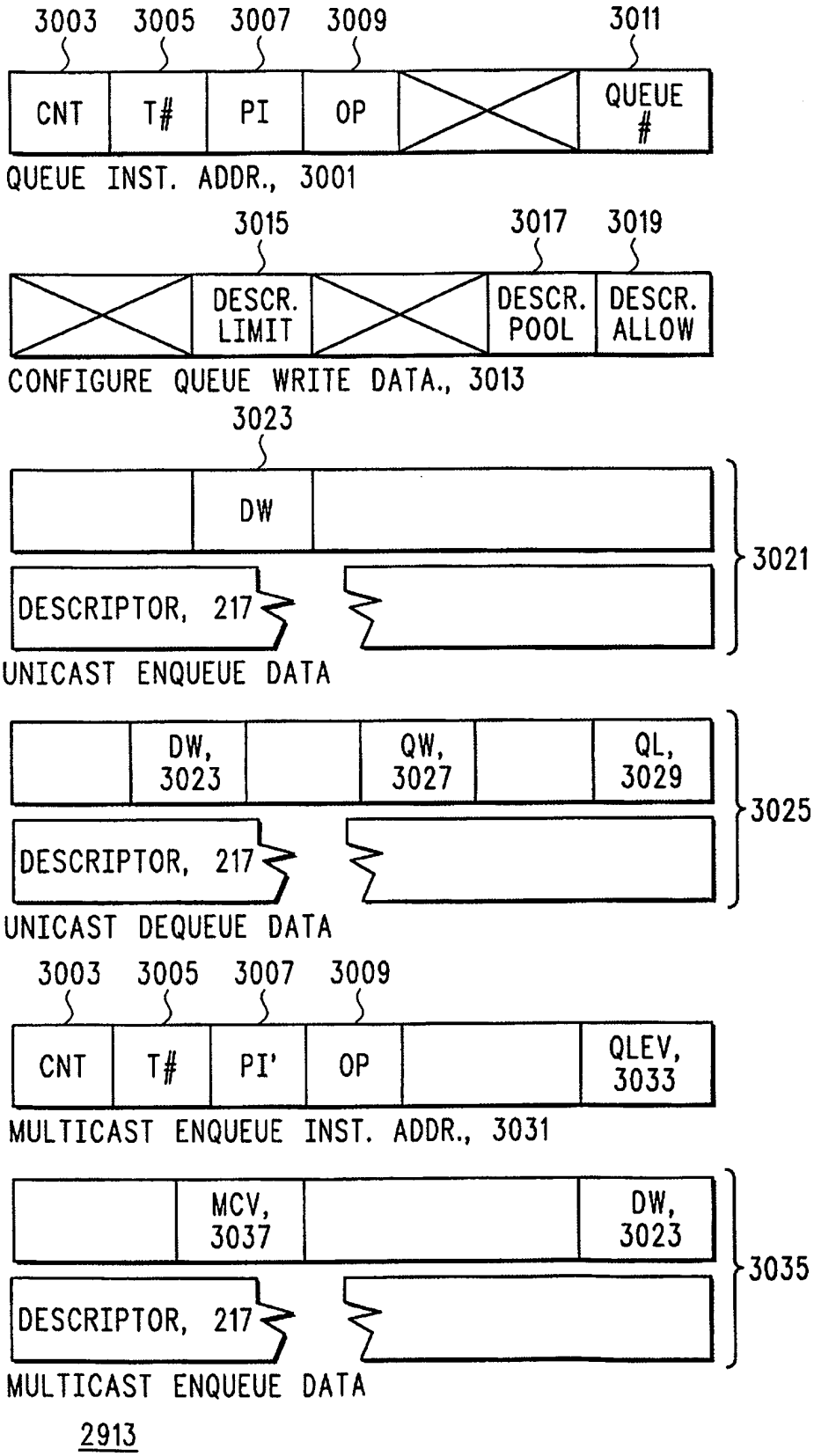


Fig. 30

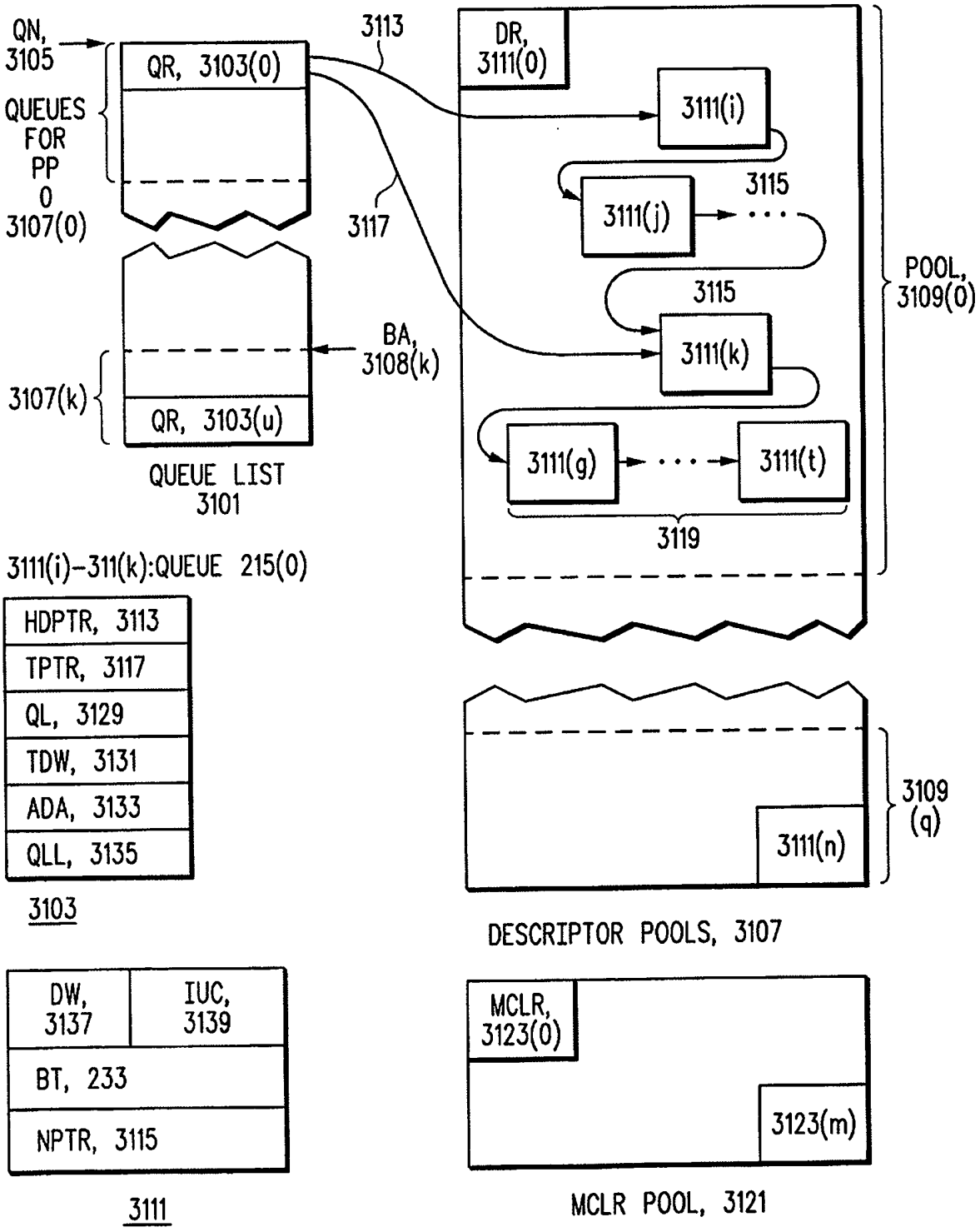


Fig. 31

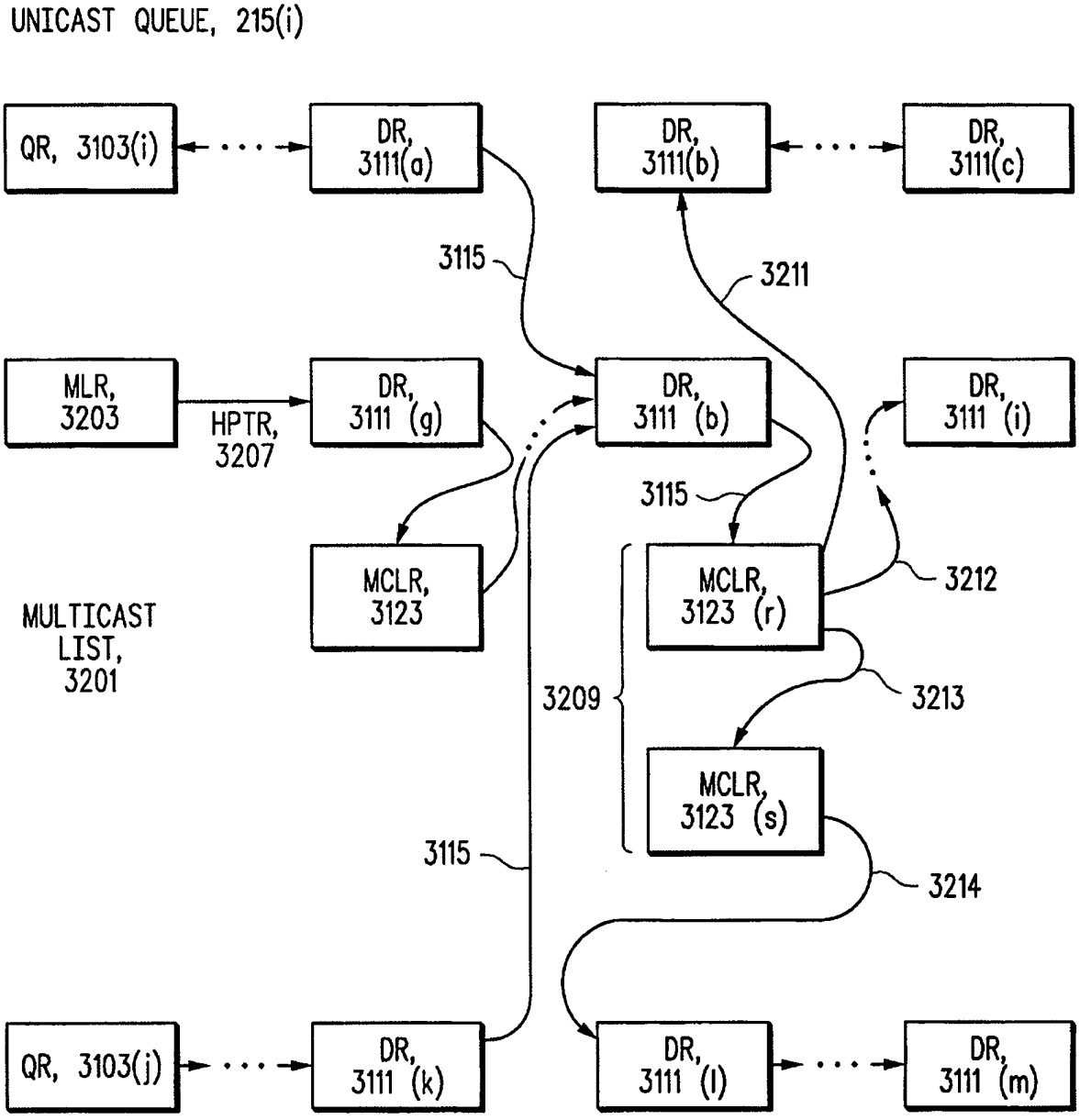


Fig. 32

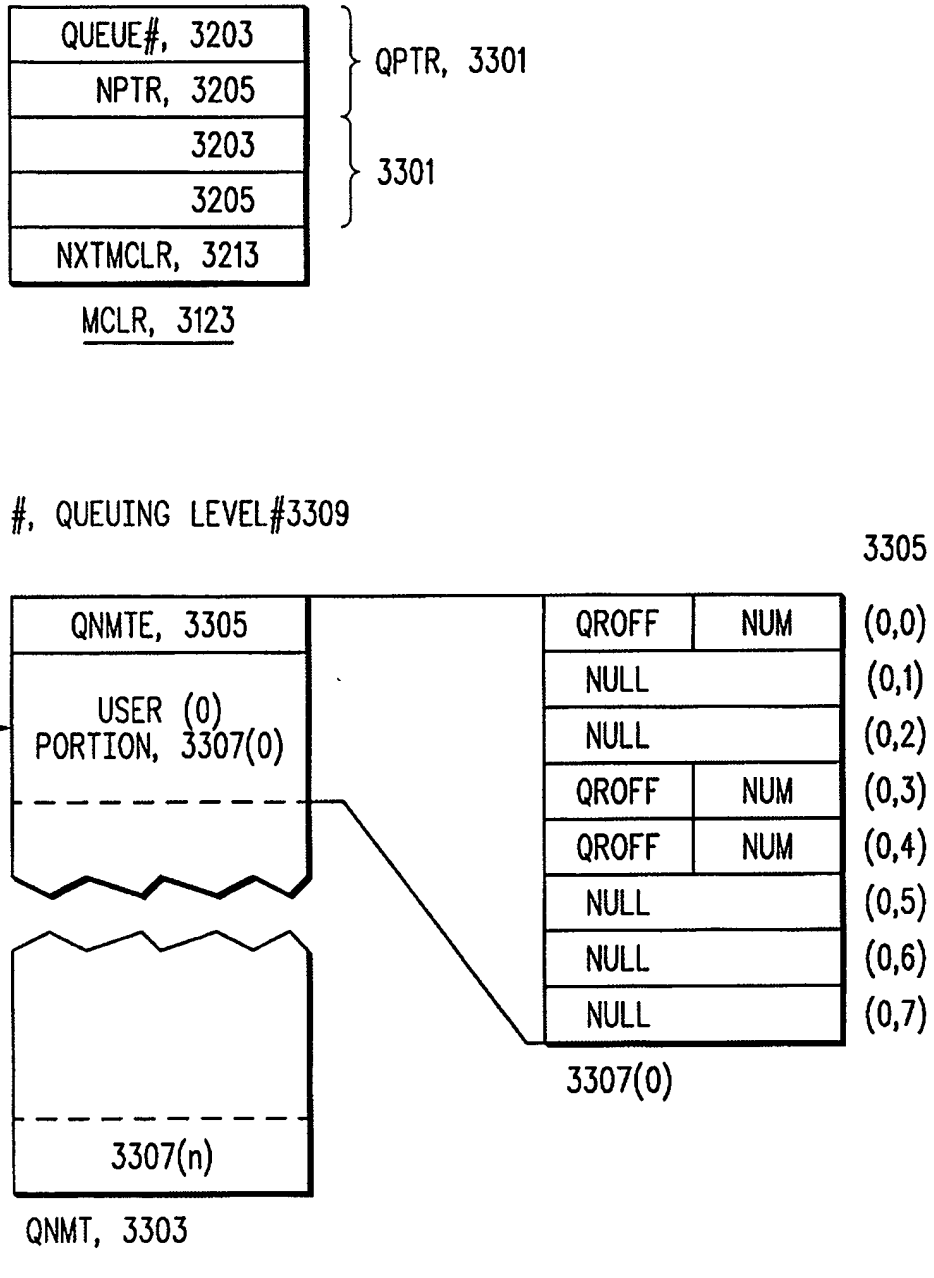


Fig. 33

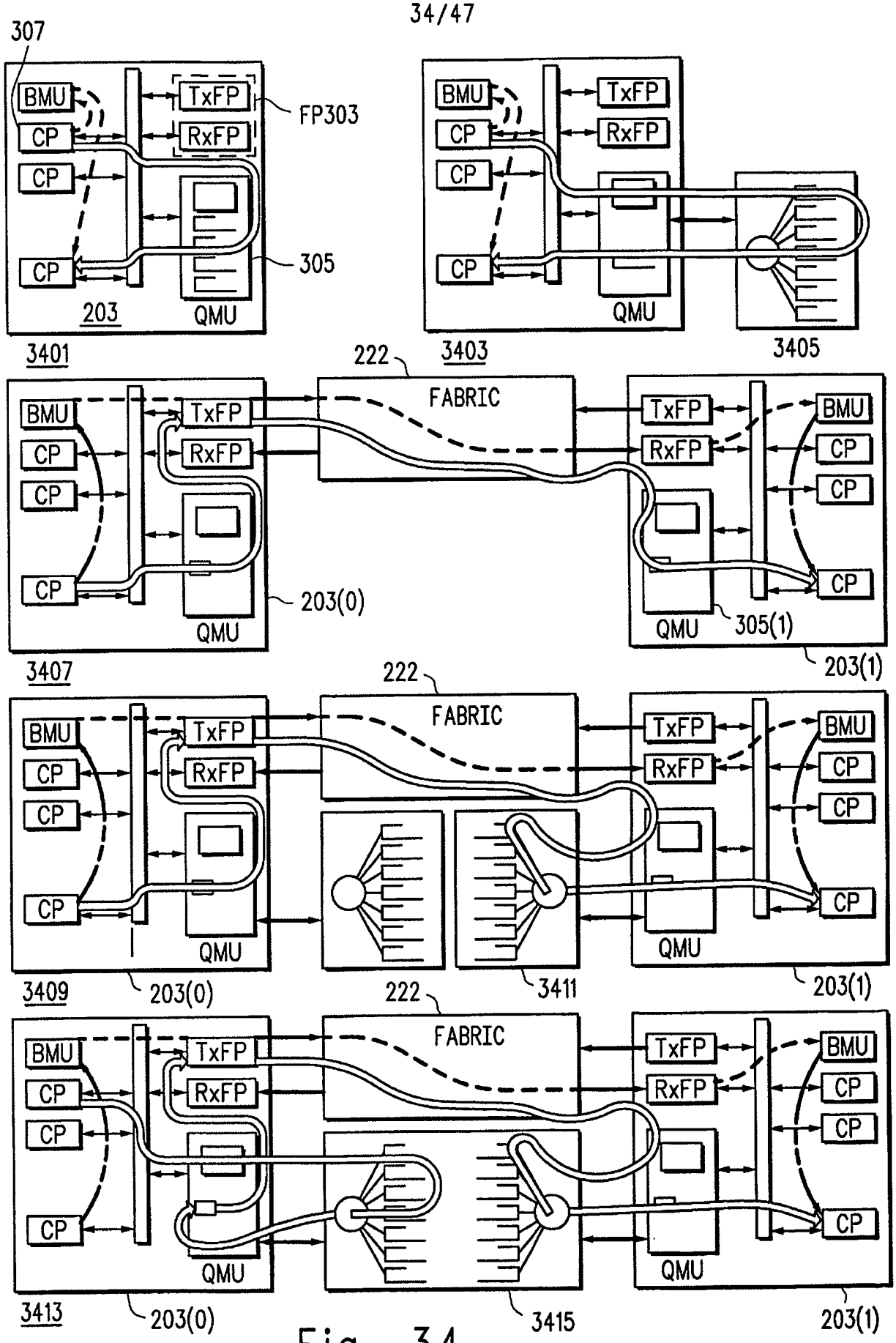


Fig. 34

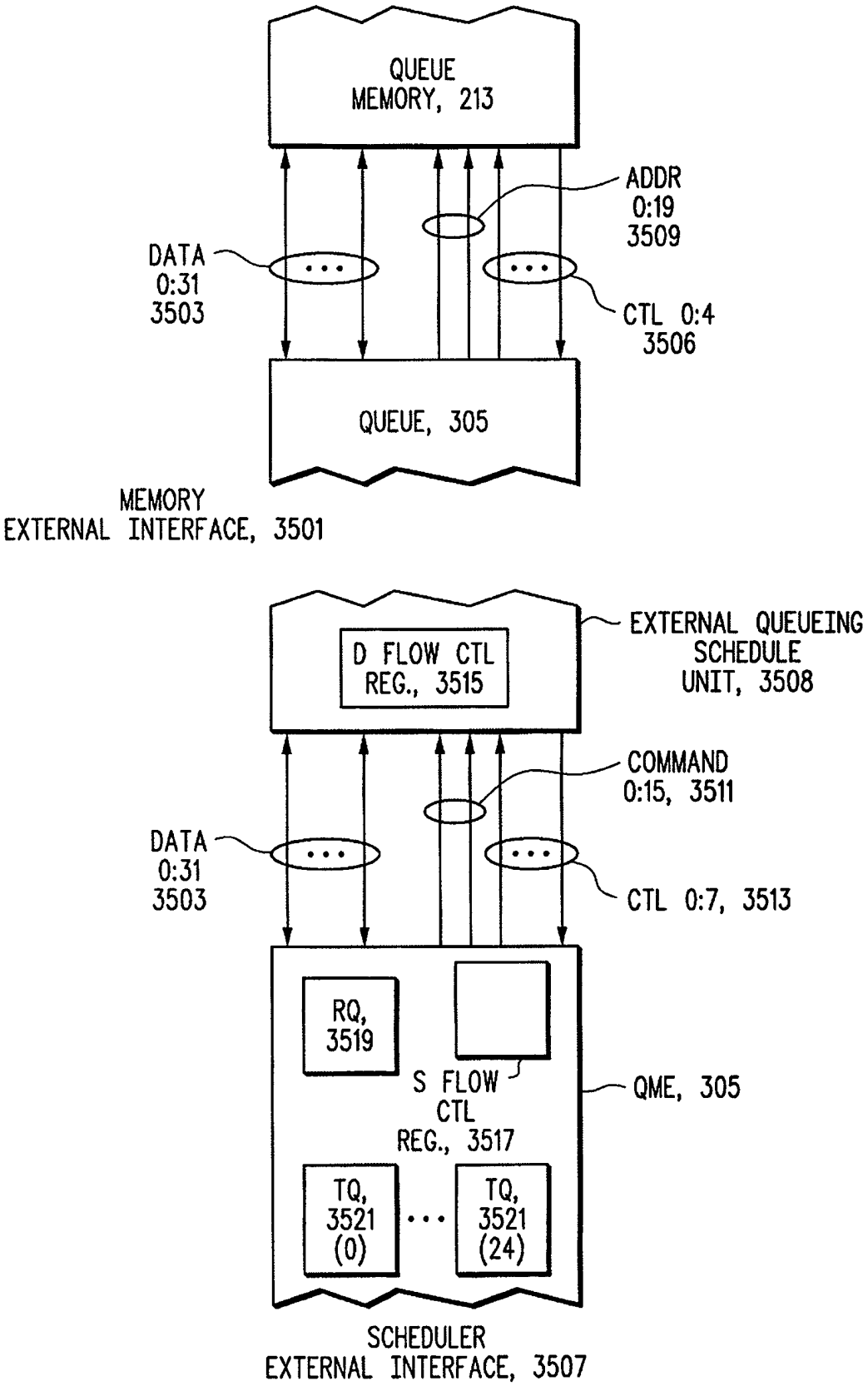
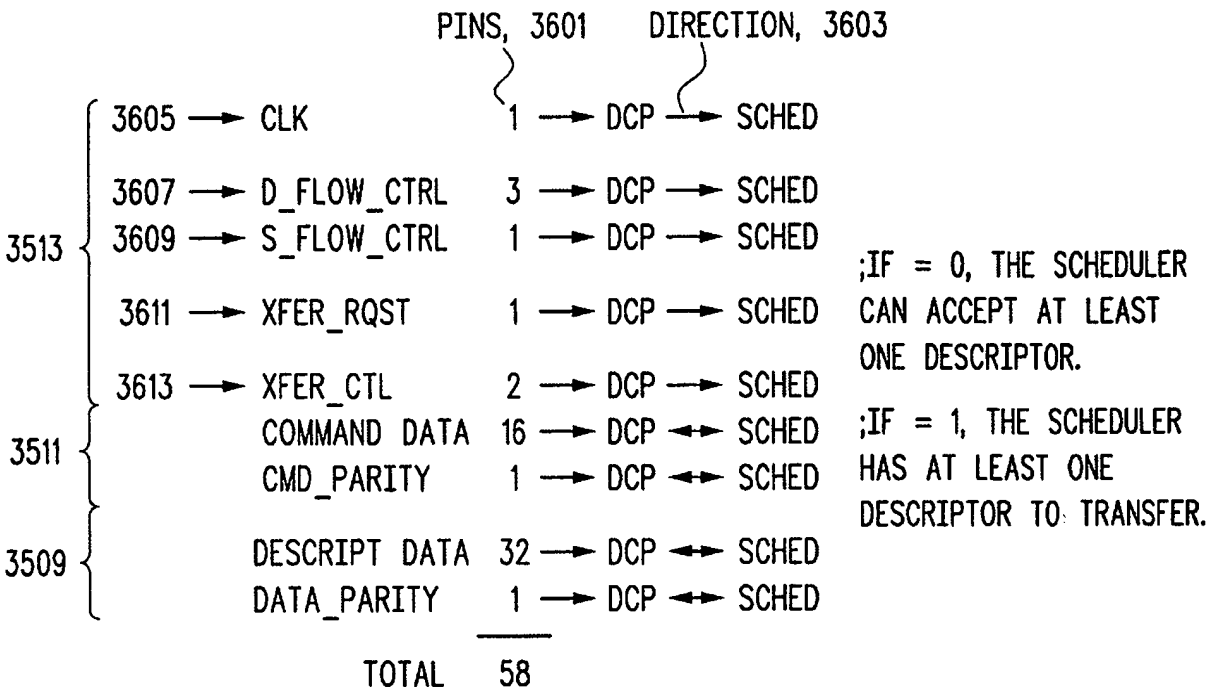
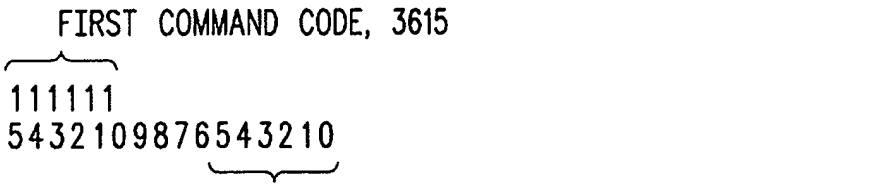


Fig. 35



3507



3514

Fig. 36

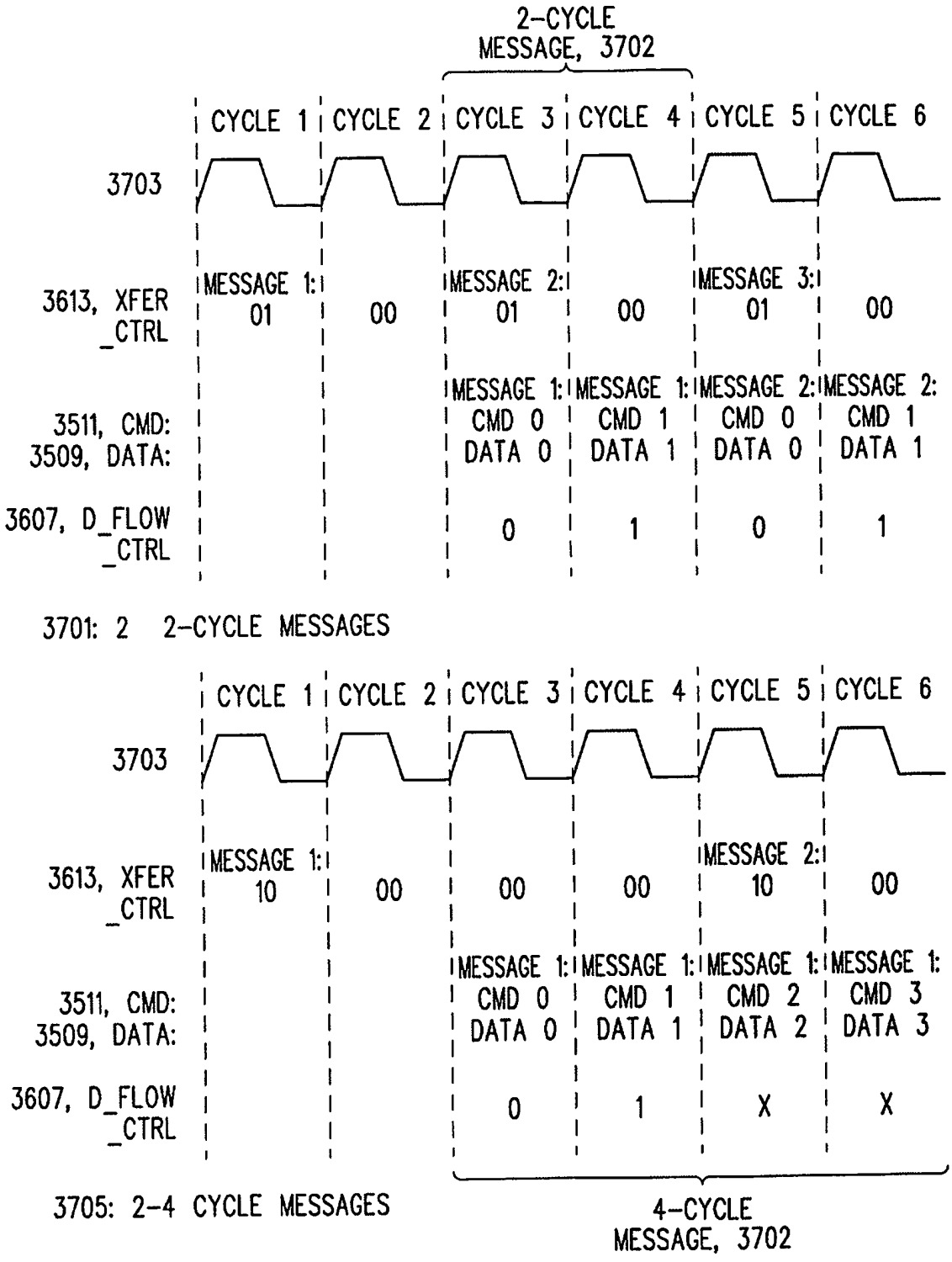


Fig. 37

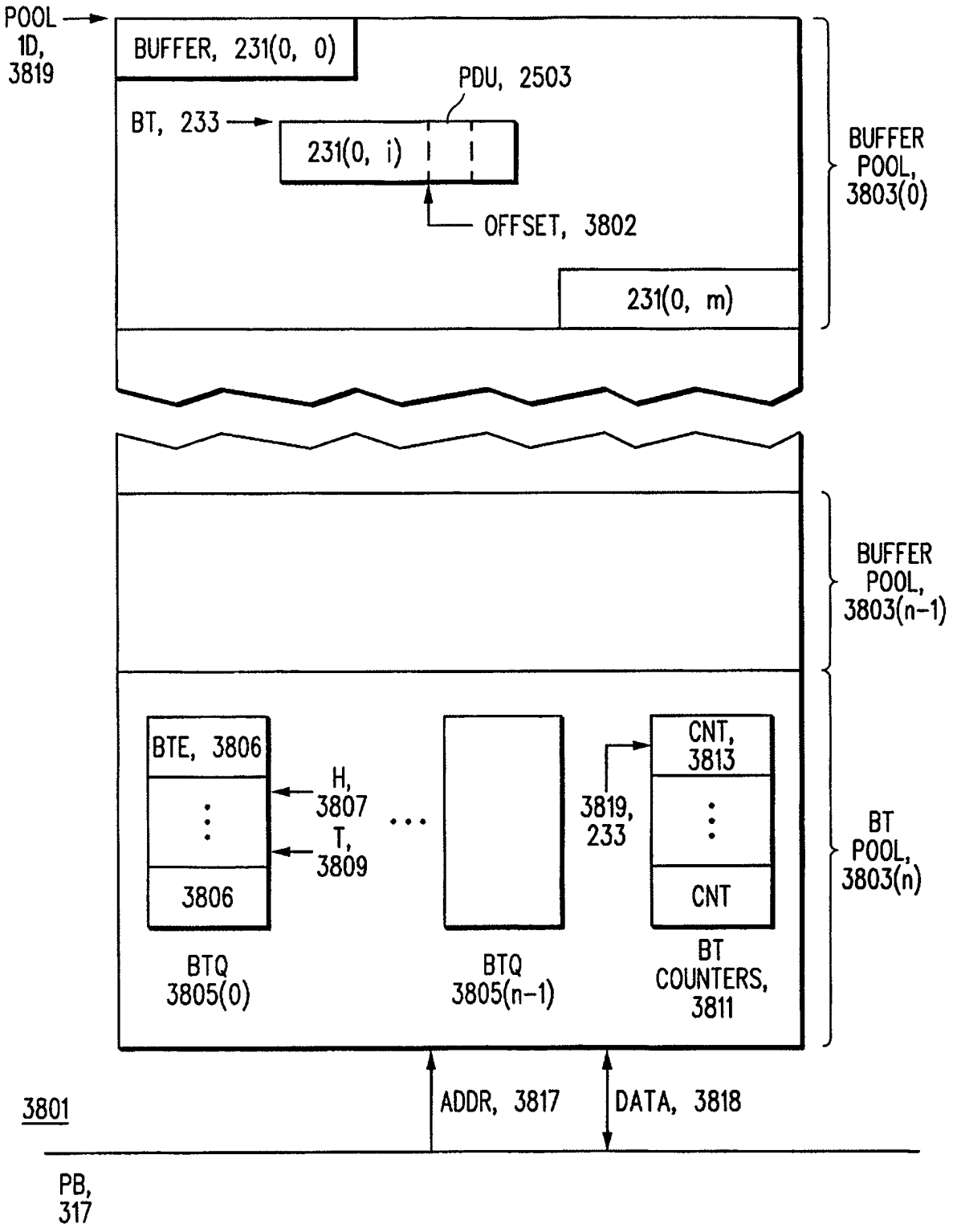
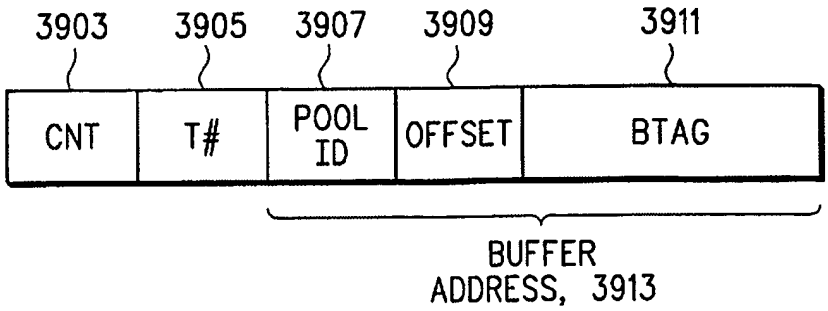


Fig. 38



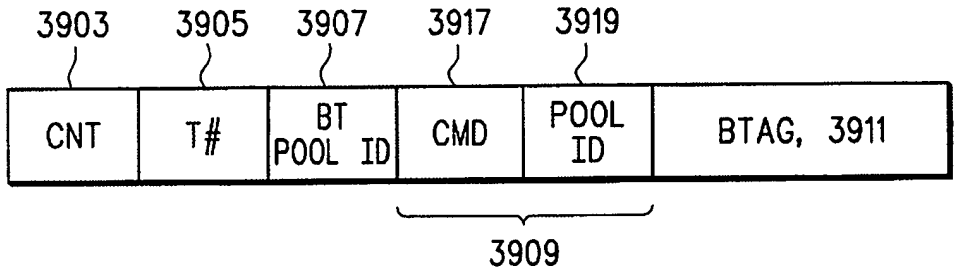


Fig. 39

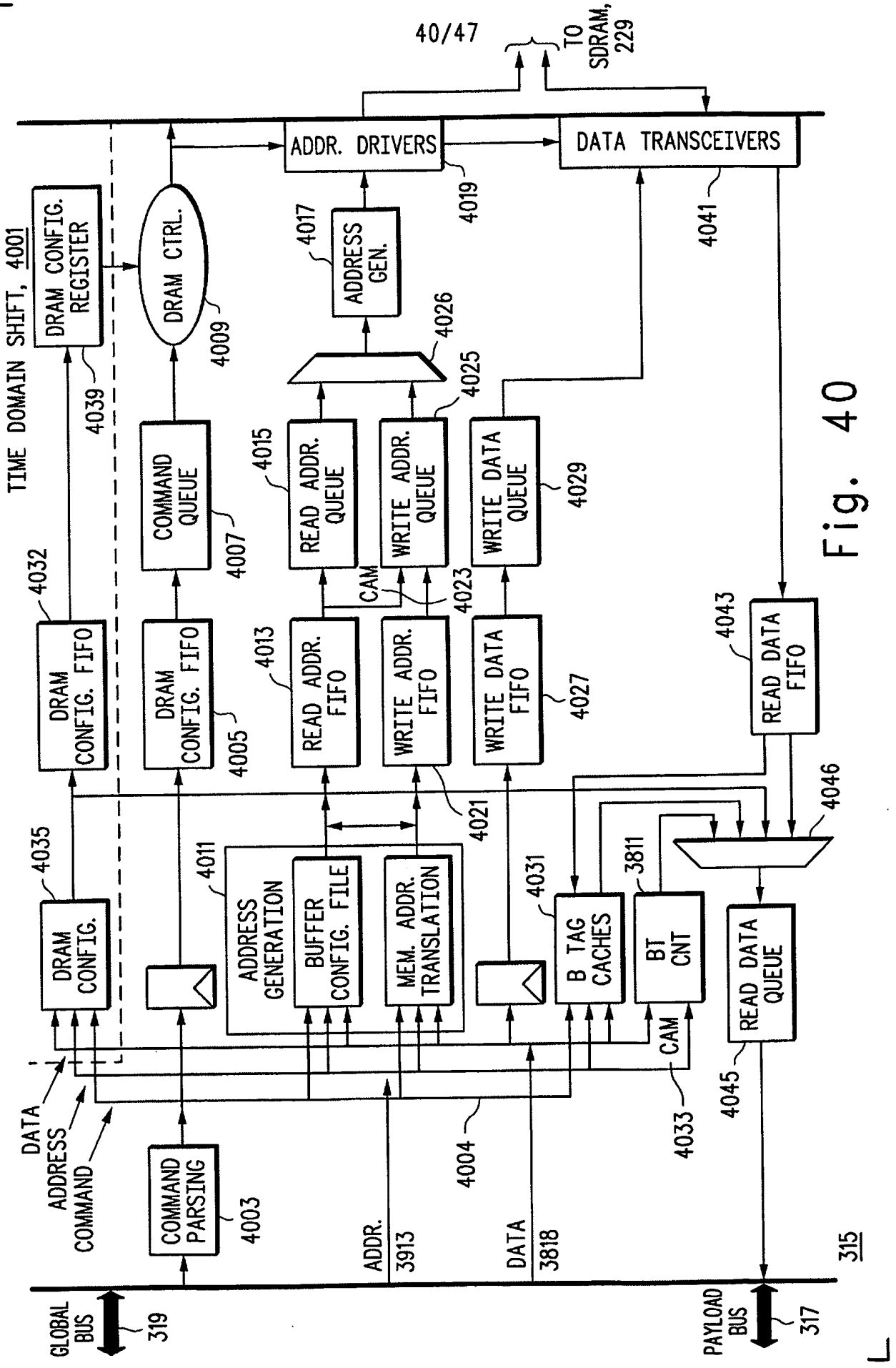
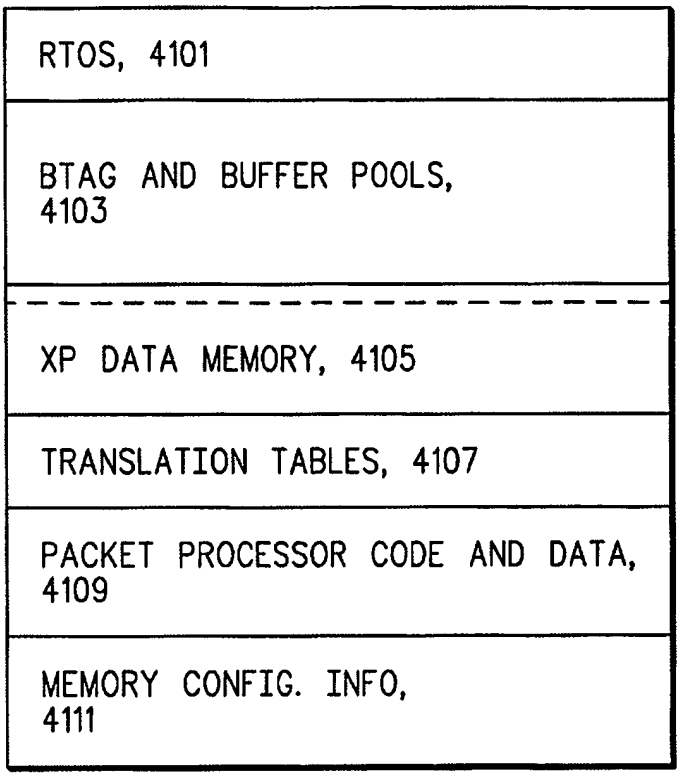
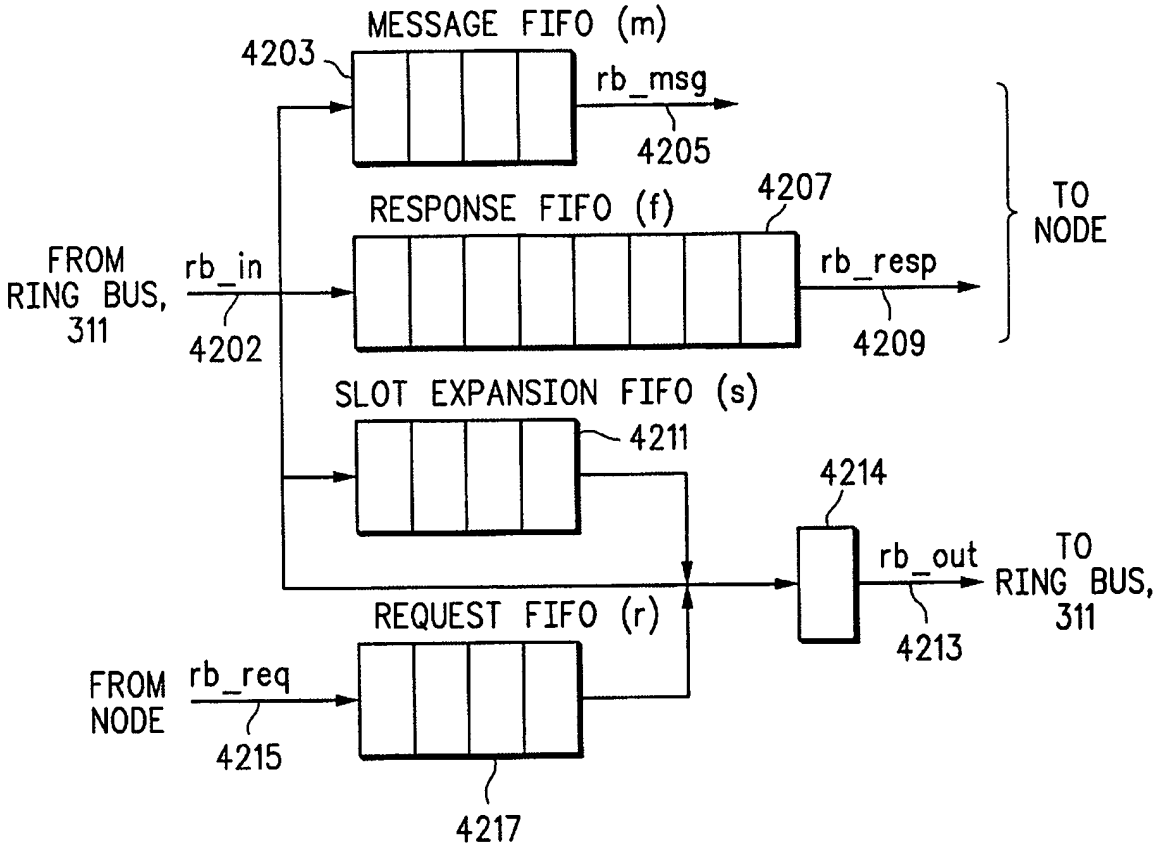


Fig. 40



229

Fig. 41



RING BUS
NODE INTERFACE, 4201

Fig. 42

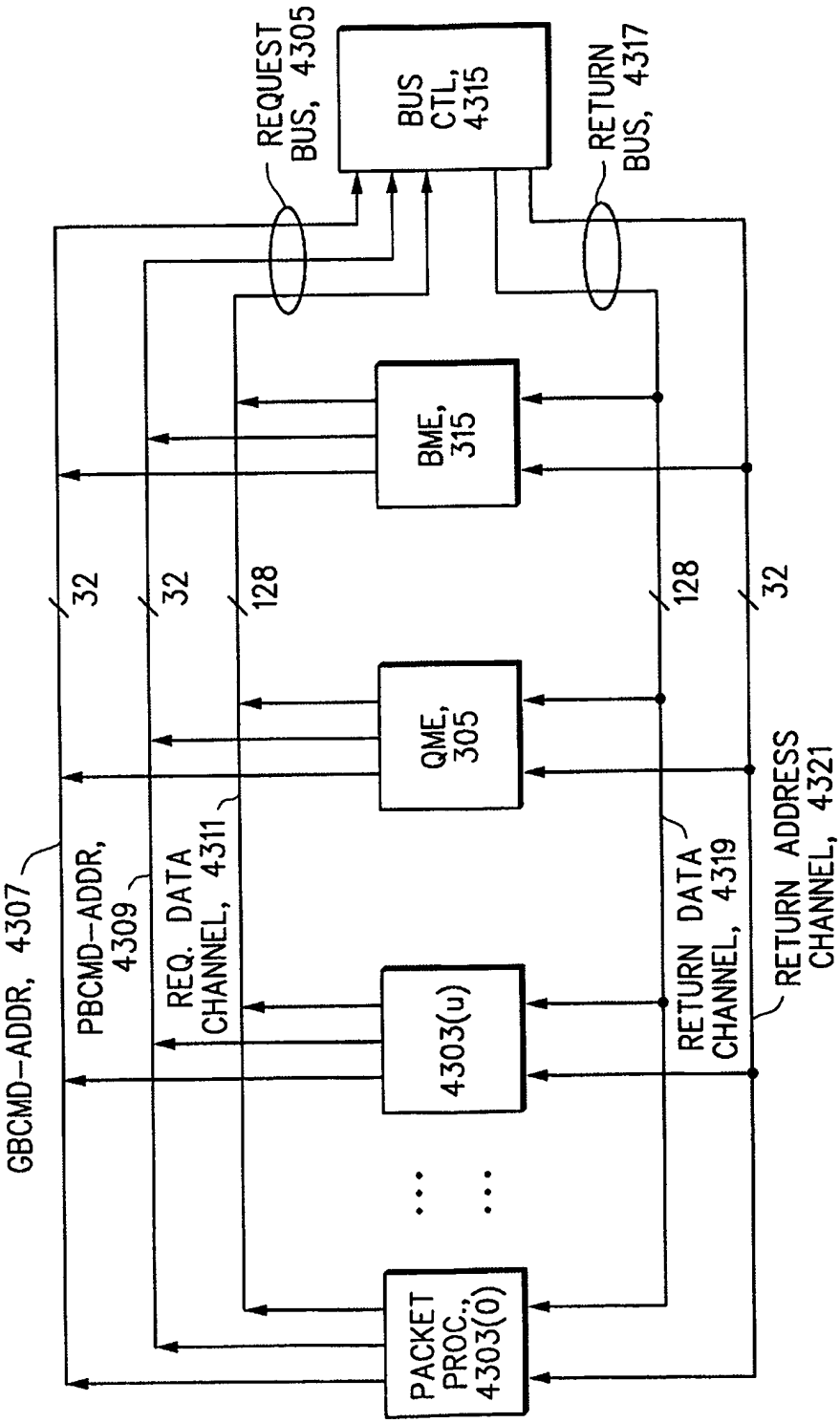


Fig. 43

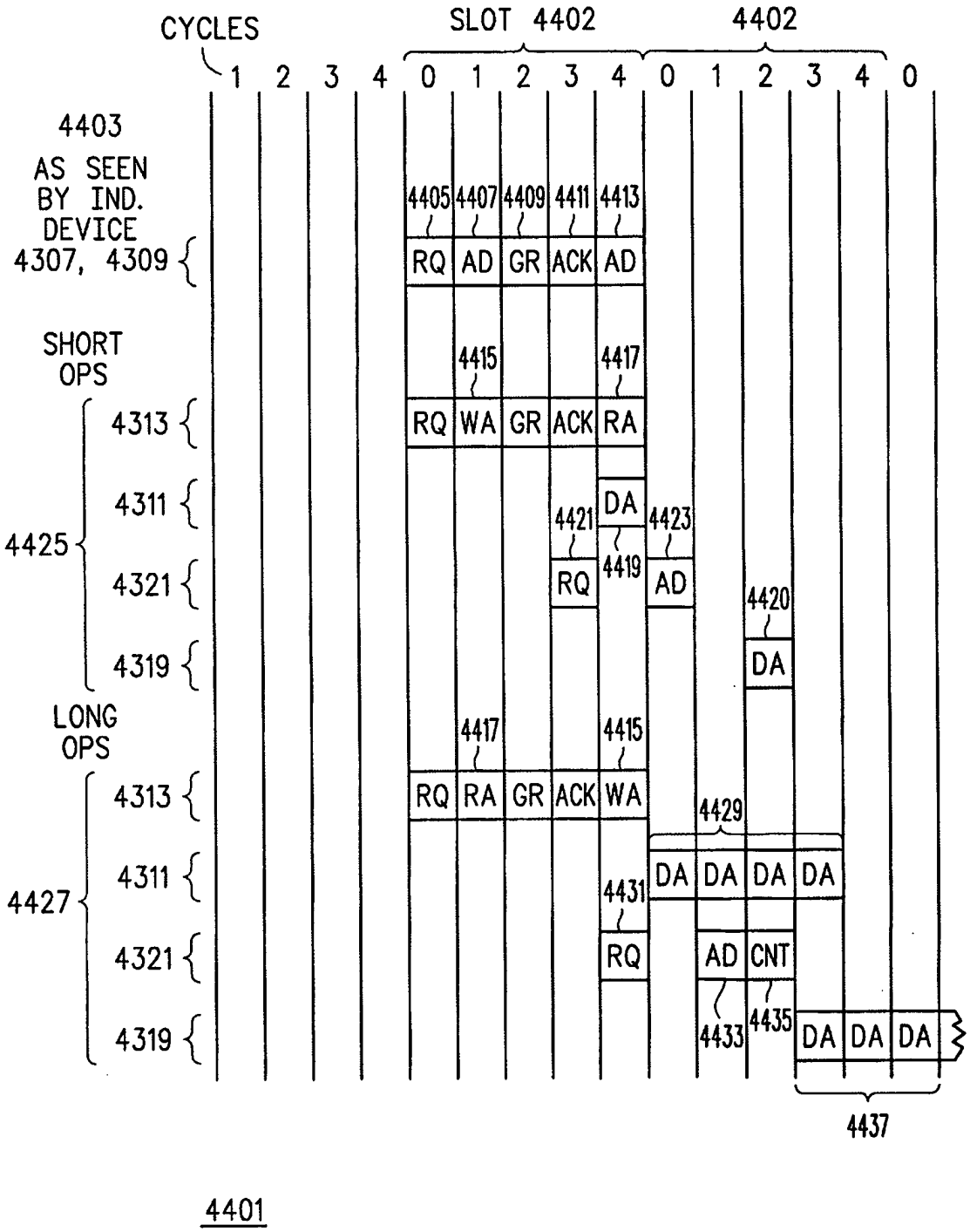
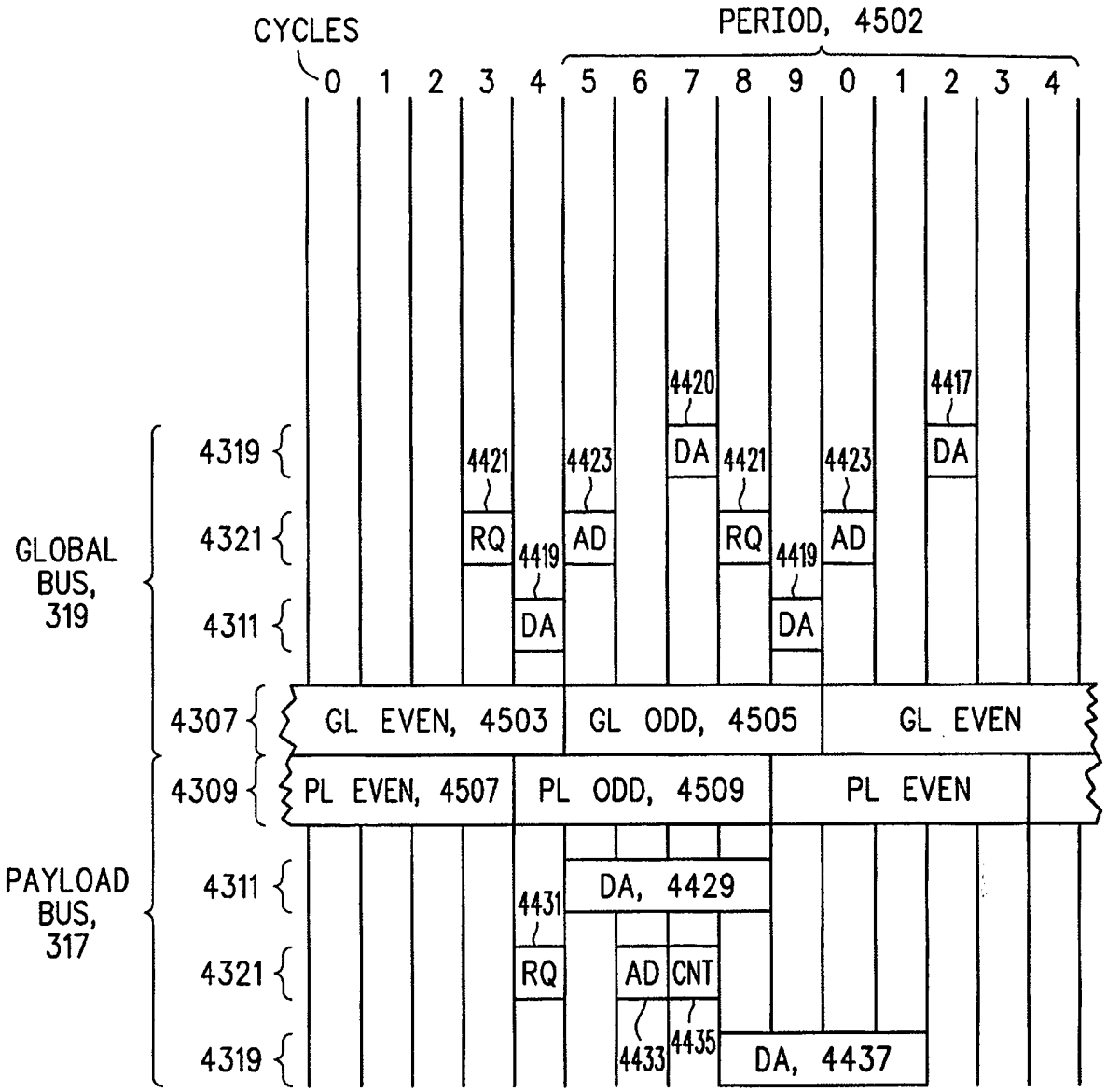


Fig. 44



4501

Fig. 45

4603	4605	4607	4609	4611	4613	4615		4617		4619
PIN	PURPOSE	RMII	OC-3	DS1	DS3	GMII (Tx)	GMII (Rx)	TBI (Tx)	TBI (Rx)	OC-12
CP0_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK	TCLK	nc	TCLK	nc	TCLK
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	CRS	nc		nc	TCLK1
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	TXD(0)	nc	TXD(0)	nc	TDX(0)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	TXD(1)	nc	TXD(1)	nc	TDX(1)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	TXD(2)	nc	TXD(2)	nc	TDX(2)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	TXD(3)	nc	TXD(3)	nc	TDX(3)
_6	DATA	TX-EN	SIGNAL_DET			TX_EN	nc	TXD(4)	nc	
CP1_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	COL	nc			
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	TXD(4)	nc	TXD(5)	nc	TDX(4)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	TXD(5)	nc	TXD(6)	nc	TDX(5)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	TXD(6)	nc	TXD(7)	nc	TDX(6)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	TXD(7)	nc	TXD(8)	nc	TDX(7)
_6	DATA	TX-EN	SIGNAL_DET			TX_ER	nc	TXD(9)	nc	
CP2_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	nc	RCLX	nc	RCLK	RCLK1
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	nc	RXD(0)	nc	RXD(1)	RDX(0)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	nc	RXD(1)	nc	RXD(0)	RDX(1)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	nc	RXD(2)	nc	RXD(2)	RDX(2)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	nc	RXD(3)	nc	RXD(3)	RDX(3)
_6	DATA	TX-EN	SIGNAL_DET			nc	RX_DV		RXD(8)	FP
CP3_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK			nc	RCLKN	
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	nc	RXD(4)	nc	RXD(4)	RDX(4)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	nc	RXD(5)	nc	RXD(5)	RDX(5)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	nc	RXD(6)	nc	RXD(6)	RDX(6)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	nc	RXD(7)	nc	RXD(7)	RDX(7)
_6	DATA	TX-EN	SIGNAL_DET			nc	RX_ER	nc	RXD(9)	LOCKDET

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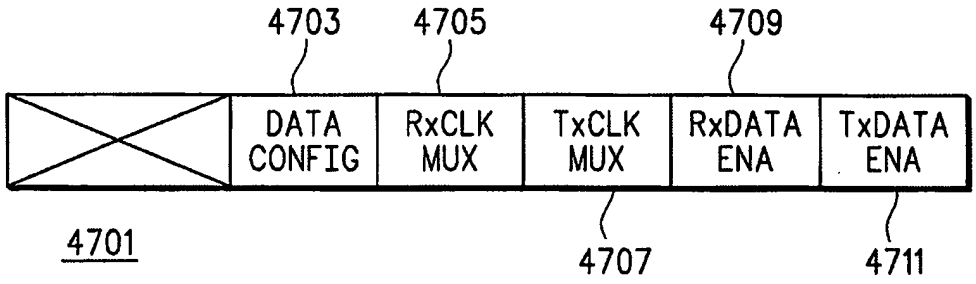
Fig. 46



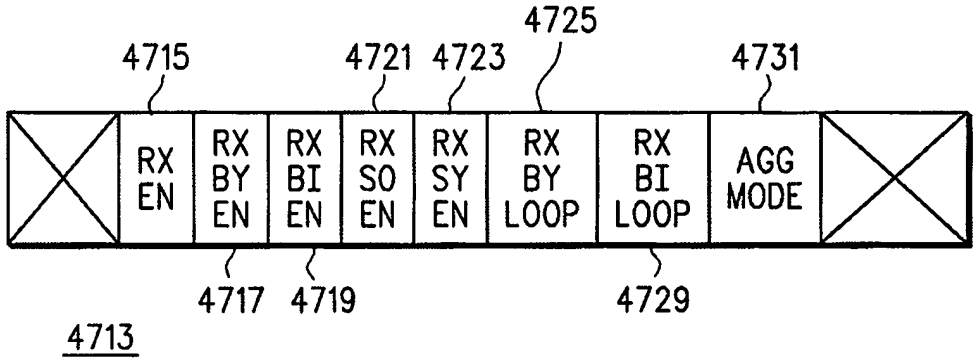


Fig. 47